Status of the Korean R&D Program on the ITER Coil Power Converters

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Abstract. Korean Domestic Agency has been performing 2-staged converter R&D to establish the technical basis for the procurement package of ITER AC/DC converter. The first phase R&D demonstrated the main features of ITER converter such as the current sharing of 1.28 and FSC (Fault Suppression Capability) at the peak current level of 175 kA with a 1/6-scaled ITER VS converter. The second phase R&D is to build 1/2-scaled ITER converter that realizes the full integration of all assemblies. The structure safe from severe electromagnetic stress under high fault current level up to 300 kA will be engineered and verified.

1. Introduction

The ITER coil power supplies are the AC/DC converters that provide voltage/current to the superconducting magnets (TF, CS, PF VS, CC coils), of which technology is assumed to be the thyristor technology due to the high demand of current capacity and high voltage together. Korea is responsible for the procurement package of ITER AC/DC converter that is shared between Korea (38%) and China (62%). Its procurement arrangement (PA) is planned on December 2010.

In order to demonstrate the feasibility of FDR2001 baseline design [1], ITER team carried out the prototype R&D by using 4-inch thyristors in 1998 [2]. The collaborative activities among ITER Organization (IO) and Domestic Agencies (DAs) under the frame of the Integrated Product Team (IPT) for the improvement and stabilization of the FDR2001 design are underway since 2008. The main issues of the FDR2001 design are the system stability due to the huge amount of reactive power, the reliable operation of the bypass mode, and the engineering improvement of unit configuration.

The uncertainties and the lack of detail information in FDR2001 baseline design are high risk to the DAs' procurement. A certain effort to investigate the technical issues and improve the design solutions is definitely required in this sense. The strategic converter R&D program for the ITER coil power supply was prepared by two-staged stepwise approach (R&D-1 and R&D-2) to verify the design concept and technical issues for the realization of the final configuration of ITER converters in Korea. As recommended in the FDR2001, 5-inch thyristors are adopted and engineered in this R&D program.

2. Design Concept of First Phase Converter

In the first phase R&D (R&D-1), the experimental verification on the main features of the ITER converters with 5-inch thyristors was aimed through the design and test of the 1/6-scaled ITER VS converter with the topology of a single-phase rectifier as shown in figure-1. The main features are the current sharing among 8-thyristors in parallel under both normal and fault conditions, and the FSC as protection criteria under very high fault currents. The rated

DC output current of the R&D-1 converter is 11.25 kA with a FSC level at the peak short circuit current of 175 kA. Table-I shows the key parameters of R&D-1 converter.

The design concept of a new converter structure addresses the reliability of the essential components such as thyristors and fuses under the ITER-like specific cyclic loads for 20 years. The homogeneous contact between the thyristors and its mating surfaces during such a long life should be assured in the concept design. The effective cooling of heated thyristors to limit the junction temperature within the safe limit is also a key concern. In addition, the overall structure design is re-evaluated to improve the accessibility and the ease of the replacement of the failed devices. The 12-pulse converter unit is made by two 6-pulse converter module. Each module is modularized by the same type of bridge arm. The distance between arms is wide enough for the human access for the maintenance. The AC inputs are connected to the middle bus-bar terminals of each arm. For the back-to-back bridge configuration in a 6-pulse converter module, upper/lower-side bridge structure or front/rear-side bridge arms can configure the inverter unit.

TABLE I: KEY PARAMETERS OF R&D-1 CONVERTER.

6 Pulse Converter Rating	Max. Load Voltage: 1.55 kV DC Current: 11.25 kA Converter Capacity: 24 MVA
Maximum Fault Current	175 kA
Number of Thyristors per arm	7+1
Thyristor Type	Infineon T4021N (5 inch)
Thyristor Specifications	Peak Forward/Reverse Voltage: 5.2 kV Average Current: 3.9 kA Maximum Transient Surge Current: 105 kA

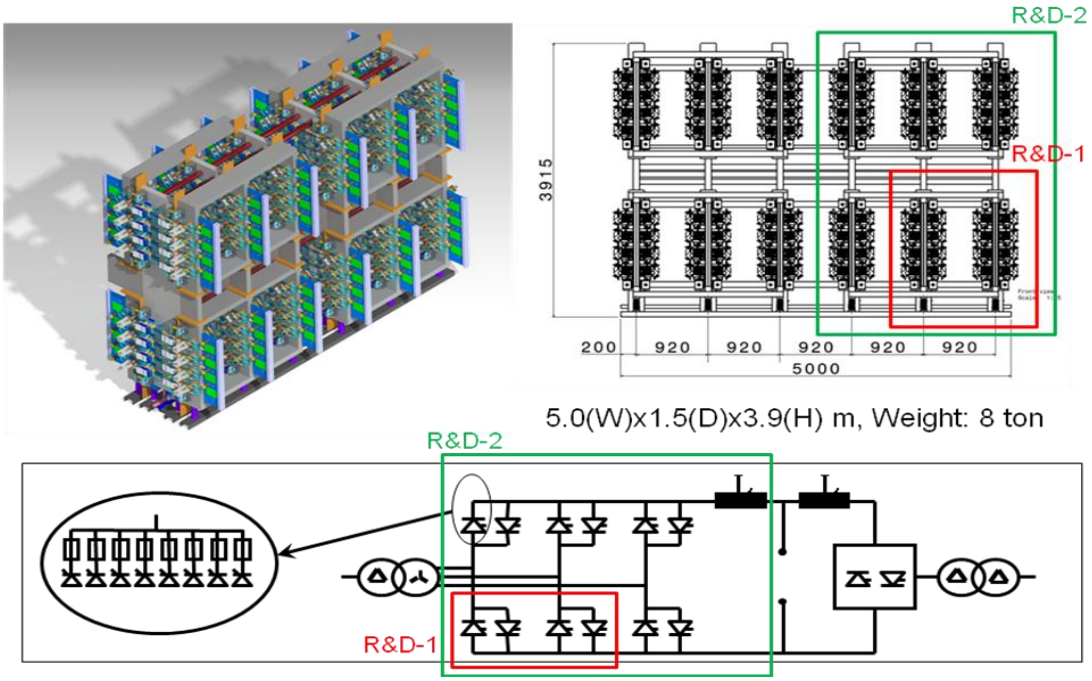


FIG. 1. Staged R&D Plan of ITER Converter in Korea.

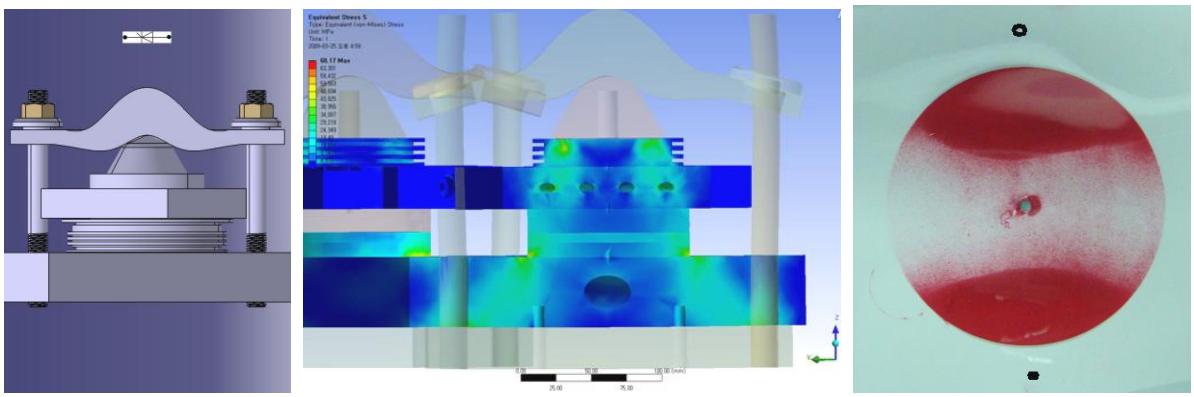


FIG. 2. Single-Sided Clamping Structure (Left), Pressure Analysis (Center) and Measured Pressure Distribution (Right) of FDR2001 Design.

2. Design Details of First Phase Converter

The suitable clamping structure for 5-inch thyristors with homogeneous and stable contact between thyristors and heat sink structures was engineered through the analytical evaluation of the pressure distribution of the structure and the verification using a pressure sensitive film (Fujifilm Prescale). First, the mockup of the clamping structure adopted in the FDR2001 design was fabricated to examine the soundness of the design suitable for 5-inch thyristor. It was proved difficult to provide the homogeneous pressure over the contact surface due to the deformation of the base bus bar along the clamping bolts as shown in the figure-2.

After the exercise of the FDR2001 clamping design, a new clamping structure is devised as shown in the figure-3 (left). By adopting double-sided mounting structure, the new design is free from such deformation in the FDR2001 design because there are only compressing forces from both sides through the clamping structure. The figure-3 (right) shows the uniform pressure distribution over the contact surface within 15% deviation. In addition, two water-cooled plates attached to both sides of a thyristor can effectively remove the heat generated in the thyristors. The new arrangement naturally makes total length of the bus bar half compared to the one of the FDR2001 design, and the resistance of the bus bar becomes smaller accordingly. The symmetric and compact structure helps to improve the current sharing between the thyristors in parallel of each arm.

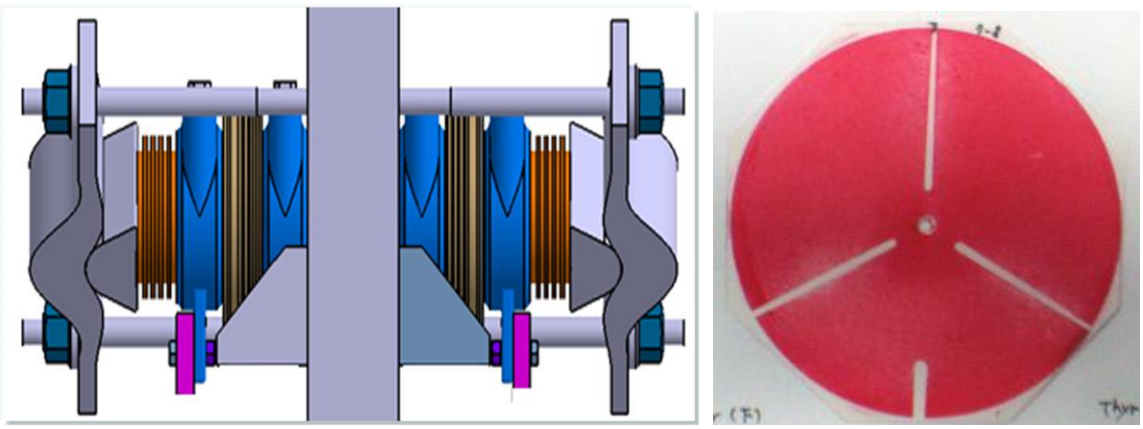


FIG. 3. Double-Sided Clamping Structure (Left) and Measured Pressure Distribution (Right) of a New Design.

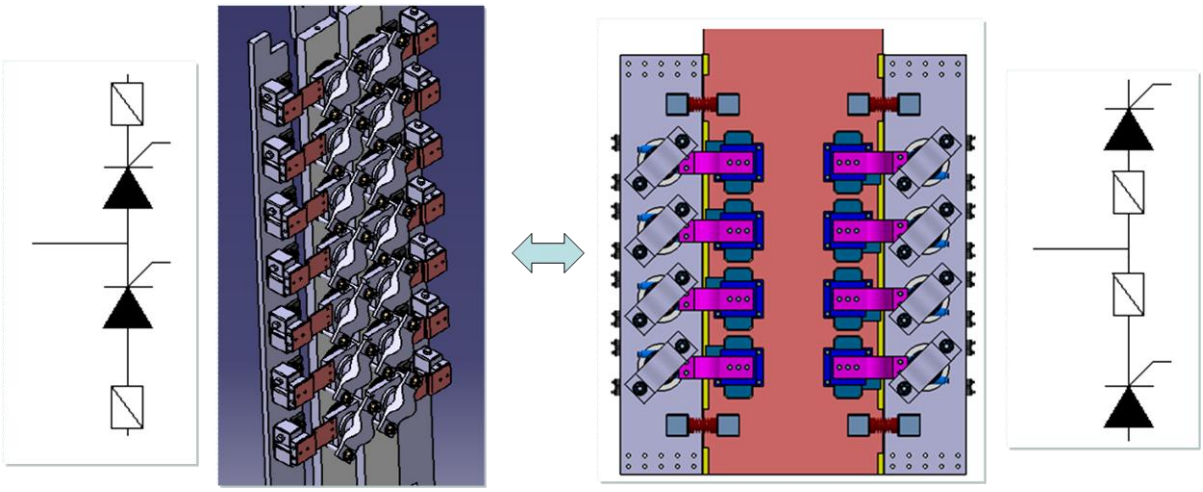


FIG. 4. AC/DC Bus Structure for FDR2001Desing (Left) and New Design (Right).

The AC/DC bus structure is also modified as shown in the figure-4. Under severe electromagnetic interference environment, short connection lead wires between gate drivers and thyristors are highly recommended. Therefore, thyristors and fuses are swapped and thus thyristors are mounted on the DC bus bars along which the gate drivers are closely mounted. The two separated AC bus bars in the FDR2001 design are combined into one wide AC bus bar that provides better conductance and current distribution. The connecting bus bars between thyristors and fuses are changed from rigid cupper to flexible aluminum to absorb the mechanical stress possibly applied to the fuses due to the thermal expansion of bus bars.

Figure-5 shows the photograph of the fabricated R&D-1 converter. It is 1/6 scale of full 12-pulse converter. It is configured as a single-phase thyristor rectifier to operate and test the dynamic characteristics by current flow through the thyristors and fuses. The overall size of the structure is 2.1 m (width) x 1.5 m (depth) x 2.7 m (height) and its weight 2.5 ton. The AC inputs are connected to the AC bus bars from top-side and the DC outputs to the DC bus bars from bottom-side. Two arms are mounted on the high-voltage epoxy insulator supports. The insulator rods combining two arms enhance the mechanical strength to withstand the strong electromagnetic force under the high surge current due to the short circuit.

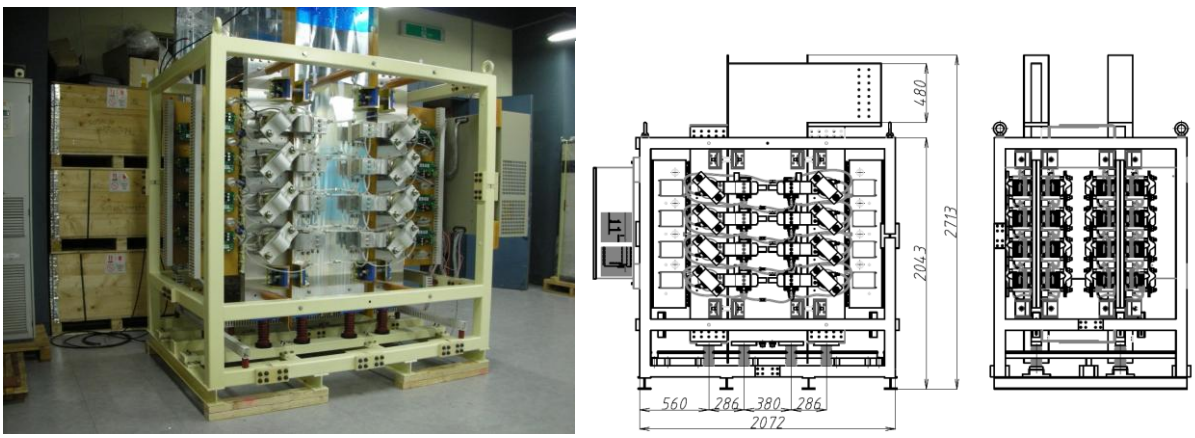


FIG. 5. Photograph of a R&D-1 converter (Left) and its sectional view (Right).

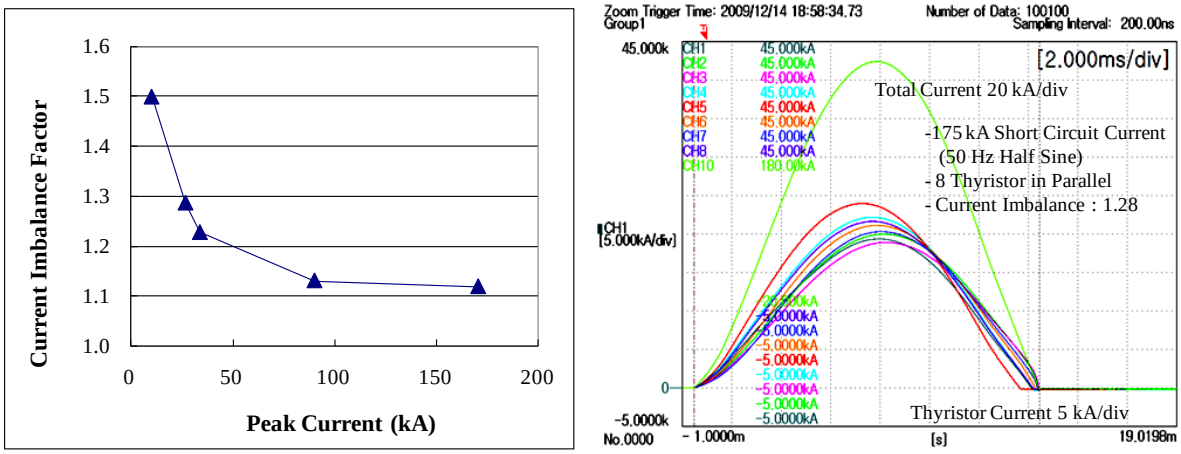


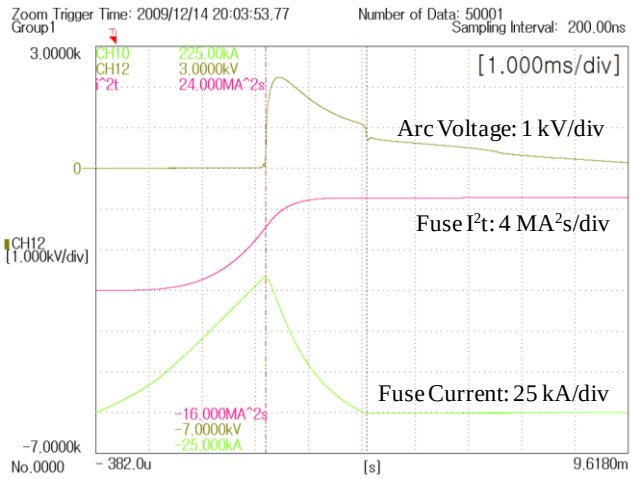
FIG. 6. Current Imbalance vs. Peak Current (Left) and Fault Current Waveform of Parallel Thyristors in an Arm of R&D-1 Converter (Right).

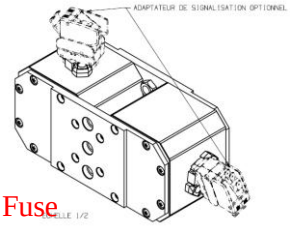
3. Test Results of First Phase Converter

The current sharing characteristic of parallel thyristors is sensitive to the turn-on characteristics of thyristor device itself. The turn-on voltage of thyristors (Infineon T4021N) is distributed from 1.62 V to 1.77V and they are classified into 4-groups having bandwidth less than 40 mV. The steep-rising current waveform of a gate driver is provided so that the measured gate turn-on delay time is confirmed to be less than 2 micro-second and the its jitter is less than 0.2 micro-second. Additional control of current balancing is assisted by two kinds of aluminum bas bar having different length, which connect fuses and thyristors.

The measured current sharing characteristic as a function of peak current is shown in the figure-6 (left). The current imbalance factor (maximum current divided by average current) is getting better as the current level increases. It is because the turn-on voltage drop of the thyristor is non-linearly increasing as current does. The current imbalance at the fault current level of 175 kA was confirmed 1.28 which satisfies the ITER requirement (<1.4). The detailed current waveform of paralleled 8-thyristors in an arm at the fault condition is measured as shown in the figure-6 (right). Therefore, once the current balancing is good enough at rather lower level like a normal operation, it is safe to keep the better current sharing at the higher current level.

The FSC (Fault Suppression Capability) criteria requests that the fuse should melt only in the case of thyristor failure in FDR2001. During the current imbalance measurement, it is already confirmed that the fuses are not affected by such high surge current. The thyristor failure is simulated by turning only one thyristor among 8-parallel ones under the same short circuit condition and the test result is shown in the figure-7. The dual-type Ferraz fuse has the working voltage of 1550 V, the working current of 2800 A, and I^2t value of 17.8 MA^2s. The measured breaking current of the fuse is 83.5 kA. It is close to the frequency-corrected specification of 80.7 kA. This value is less than the maximum transient surge current of the thyristor. In addition, there is no rupture at the fuse and the conducting thyristor under such test. The fuse melting time is 3.2 ms and the fault clearing time is 5.1 ms with the arc voltage of 2.24 kV. The net arc voltage is about 1500 V that is the corrected specification by working-voltage.





Ferraz Fuse
1550 V, 2800 A, 17.8 MA^2s

Measured Data
- Arc Voltage : 2.24 kV
- I^2t (melting) = 6.25 MA^2s
- I^2t (total) = 9.11 MA^2s
- Breaking Current = 83.5 kA
- Pre-are RMS Current = 44.1 kA
- Melting time = 3.2 ms
- Clearing time = 5.1 ms

FIG. 7. Type Test of FSC capability at the Fault Current Level of 175 kA.

4. Issues of the Second Phase R&D

Followed by successful R&D-1 for the verification of main features of ITER converters, next phase R&D (R&D-2) is ongoing in 2010 to build 1/2-scaled ITER converter that realizes the full integration of all assemblies including AC bus bars, DC bus bars, and a DC reactor. The one of key engineering issues is the converter structure with aluminum material that is safe from severe electromagnetic stress under high fault current. In addition, the suitable cooling design and the welding procedure have to be implemented in this structure. The full current at low voltage test will be performed to verify the current sharing among thyristors and the thermal design. The FSC criteria and electromagnetic stress will be tested under the peak short current level of up to 300 kA.

Acknowledgments

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The views and opinions expressed herein do not necessarily reflect those of the ITER Organization.

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