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NUCLEAR ELECTRONICS LABORATORY MANUAL

1989 EDITION

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FOREWORD

The second edition of the Nuclear Electronics Laboratory Manual is a joint product of several electronics experts who have been associated with IAEA activity in this field for many years. It is based on the experience of conducting twenty three training courses on nuclear electronics. In this respect, the contribution of many other scientists, and participants in these courses, are implicitly present in the final manuscript. The first edition was published in 1984, and was used in a number of training courses on interregional regional and national level. The deficiencies of the first edition are to a large extent corrected in the present version. Many new experiments have been added, mainly on the advanced technical level.

The manual does not include experiments of a basic nature, such as characteristics of different active electronics components. It starts by introducing small electronics blocks, employing one or more active components. The most demanding exercises instruct a student in the design and construction of complete circuits, as used in commercial nuclear instruments. It is expected that a student who completes all the experiments in the manual should be in a position to design nuclear electronics units and also to understand the functions of advanced commercial instruments which need to be repaired or maintained.

The future tasks of nuclear electronics engineers will be increasingly oriented towards designing and building the interfaces between a nuclear experiment and a computer. The first edition of the manual outlined these developments by introducing a number of experiments which illustrate the principles and the technology of interfacing. However, it was found that the complex topic of interfacing is too broad (and too important) to be covered in a superficial manner in the nuclear electronics manual. Therefore, the topic of interfacing is not included in the second edition. Instead, the IAEA will publish a separate manual dealing exclusively with the problems of interfacing in nuclear experiments.

There are two other IAEA TECDOC publications that can be considered companions to the present manual: TECDOC-363: Selected Topics in Nuclear Electronics, and TEC-DOC-426 : Troubleshooting in Nuclear Instruments. Together, these three documents cover a wide spectrum of electronics circuits, units and devices, and can be applied to training in the field of nuclear instrumentation and electronics.

ACKNOWLEDGEMENTS

The International Atomic Energy Agency has conducted training courses in nuclear electronics since 1966. For the last 15 years, this has been a regular annual course, on an advanced level. During these years, several institutions in different countries, and a number of scientists have contributed to the development of the methodology, as demonstrated in the present Manual. Only some can be mentioned below.

The Government of the Federal Republic of Germany supported the IAEA efforts in this field by sponsoring a project entitled "Development of teaching aids for training in nuclear instrumentation" in the period 1985-90.

The Divison of Educational Programs, at Argonne National Laboratory hosted three IAEA training courses in the years 1988-90. A workshop organized in Argonne in July 1989 produced the final version of the Nuclear Electronics Laboratory Manual, and was to a large extend sponsored by the Government of the USA, though the State Department.

Several engineers and scientists from many IAEA Member States have contributed to the first edition of the Manual, published in 1984. F. Manfredi (Italy), D. Camin (Argentina), J Lauwers (Belgium) and H. Kaufmann (IAEA) deserve special acknowledgement.

The present, radically revised edition of the Manual is the product of the following experts:

The experiments on power supplies were expanded and revised by A. Burr (USA) who added several new ones, and contributed to other parts of the Manual.

The digital part of the Manual was designed by J. Lopes (Portugal) who improved the old experiments. and developed a number of new exercises. His contributions are found also in the chapter on multichannel analyzers,

J. Panor (Yugoslavia) contributed to many chapters of the Manual. His didactic talent is reflected in several experiments. In particular, he signs responsible for the chapter on analog nuclear electronics, and on multichannel analyzers.

F. Clikeman (USA) was involved in preparation of experiments on radiation detectors which for the first time appear in the Manual.

J. Dolnicar (IAEA) have prepared several experiments on different topics, and has coordinated the entire activities in Vienna and the United States which produced the publication presented here.

CONTENTS

INTRODUCTION

The Laboratory Manual is intended to provide orientation in training in the field of nuclear electronics. It gives information about the principles of nuclear electronics circuits while simultaneously introducing contemporary electronics technology. It is intended for students who have a background in basic electronics.

The exercises in this Laboratory Manual can be classified in several categories:

I. Each section of the Manual starts with some basic experiments selected in a way to demonstrate the building stones of nuclear electronic circuits. Thorough understanding of these basic construction blocks is considered essential for an engineer involved in nuclear instrumentations and electronics. The completion of an experiment should require at the most three hours in the laboratory.

II. The complexity of the experiments increases in each part of the Manual until it reaches a high professional level by introducing experiments that require several laboratory sessions for completion. Advanced tools, such as a logic analyzer, are introduced.

III. Special Projects in the final part of the Manual are designed to show students how to design and construct complete electronics devices for nuclear applications. The topics for these experiments have been proposed by the students that attended the IAEA training course on nuclear electronics, during the period 1986-89. In fact, these exercises reach beyond the normal course in electronics, and produce an instrument applicable to a real nuclear experiment.

The experiments and projects in the Manual have been designed for the IAEA interregional nuclear electronics training course which is conducted on a rather advanced level, and runs for 12 weeks. In this course, about 65% of the time is devoted to practical laboratory work. It is obvious that for a shorter course on a lower technical level, appropriate exercises have to be selected, and the more complex experiments will have to be deleted.

Each experiment is introduced by an explanation of the circuit operation using physical principles. In this way, the Laboratory Manual can serve at the same time as an introductory textbook for nuclear electronics. Note, however, that another IAEA document (TECDOC 363: Selected topics in nuclear electronics), provides the theoretical background for topics treated in the present manual.

To avoid the inconvenient letters for resistivity and capacitance, a simplified notation has been selected. Resistors are described in R (ohms), K (kiloohms) and M (megaohms); 10 R means 10 ohms, 2K7 stands for 2.7 kiloohm, 1M5 is 1.5 megaohm. The values of capacitors are given in pF, nF, and uF (or μF), in the drawings also p (for picofarad) and n (for nanofarad) are used.

Most of the wiring diagrams include the values of all the active and passive components used in the design. For some experiments, only suggested values are given, challenging the students to determine and select the most suitable components themself.

It is expected that the students in nuclear electronics will learn how to design a printed board, and how to produce it. However, it would be too time consuming if every student would prepare every printed board described in this manual. Therefore, a set of masks for the boards was prepared, in support of the experiments described in the Manual. These boards are available on request.

Notes:

PART ONE

POWER SUPPLIES

Power supplies - an introduction.

Most laboratories are supplied with power in the form of 110 or 220 VAC. Unfortunately no instruments can directly use this power, so one has various forms of power supplies to change the AC to appropriate values of DC.

Power supplies are unglamorous circuits, but they are some of the most important and simplest to understand. It is fortunate that they are easy to understand; because they are the most likely circuit to fail in an instrument. A good understanding of power supplies will bring greater returns in terms of savings of time and money than an understanding of any other section of electronics.

This chapter introduces one to the familiar types of rectifier circuits and conventional linear regulators necessary to provide the very stable low voltage high current supplies demanded by modern electronics. These supplies tend to be heavy; so lighter, more efficient, but much more complicated, switching regulators are appearing with increasing frequency. Thus several experiments deal with DC to DC converters and other switching circuits.

Laboratories in areas with uncertain public electric utilities face special problems. A review of basic power engineering concepts would probably be helpful to ensure that the connections between the laboratory and the local electric lines is correct and well maintained. One experiment here involves line regulators and uninterruptable power supplies which are necessary in certain critical cases.

EXPERIMENT 1.1

RECTIFIER BOARD WITH FILTER CAPACITOR

OBJECTIVE

The objective of this experiment is to study the waveform produced by rectifier circuits and to study the effect of a capacitor filter stage.

REVIEW

A rectifier is just a diode which permits currect to go in one direction only. The trouble with using only one diode to get DC from AC is that half of the AC waveform is not used. The additional diode permits the whole signal to be used. A rectifier by itself does not produce a steady voltage because part of the time no signal is available to be rectified. Therefore, some form of energy storage device is needed to supply power when there is no input. A capacitor is the component which fullfils this requirement in the easiest manner.

Power supplies are characterized by a number of quantities, some of which are mentioned here roughly in order of importance:

- voltage output
- current capability
- ripple
- regulation
- output resistance.

Most important is the voltage output. Most power suppplies are desgned for a specific voltage output as required by the circuits to which they are supplying power.

Current capacity is the maximum current which the power supply will produce without overloading some internal components. Of course, it is perfectly all right to use any lower value of current.

Ripple is a quantity which indicates how well the AC component of the output has been eliminated. Ripple is usually measured in peak-to-peak volts.

Regulation is a quantity which indicates the degree to which the output voltage is independent of the current drawn from the power supply. It is usually expressed as a percentage according to the following formula:

$$Regulation(\%) = \frac{V_{(no-load)} - V_{(full-load)}}{V_{(no-load)}} \times 100$$

Output resistance is a quality closely related to regulation. It is the equivalent resistance which, when placed in series with a perfect battery with a voltage equivalent to $V_{(no\text{-}load)}$ will most closely reproduce the voltage versus current output curve of the real power supply. It can be calculated from the curve.

EXPERIMENT

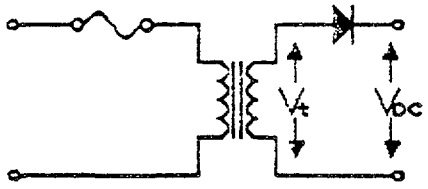
You are provided with a transformer, some rectifiers, and some capacitors.

A. Construct a half wave rectifier circuit as shown in Fig. 1.1.1.

This circuit is of limited use in power supplies, but it is used in signal detection and light duty power sources. Measure V_T and place a DC coupled oscilloscope on the output and carefully draw the output waveform.

Fig. 1.1.1:

Half-wave rectifier circuit.



If you have time, calculate the ratio of the V_T rms reading to the peak voltage shown on the oscilloscope. Study the oscilloscope trace. Is it symetric? Is the on time the same as the off time? What is the frequency of your signal?

B. Shown in the Figs. 1.1.2 and 1.1.3. are two possible full wave rectifier circuits.

Assemble one of the two possible configurations.

Measure VT and place a DC coupled oscilloscope on the output and carefully draw the output as shown by the oscilloscope. Study the oscilloscope trace carefully. Is each peak the same width? Is there any dead space between peaks? What is the frequency of the observed waveform? (It is NOT 50 or 60 Hz.)

C. Now add a filter capacitor to your circuit. Your circuit will now look like one of the Figs. 1.1.4 and 1.1.5.

Find some of the quantities which characterize your power supply.

The easiest way to obtain power supply information is to plot output voltage and ouput ripple against current drawn from the power supply. This is done by varying the R_L shown in the figures while taking data. The first quantity to find is the value of R_L to use. Clearly to get I_L small (zero) R_L must be very large (∞). To find the smallest value of R_L which can be used takes a little more work. From your previous measurments, you will note that the largest voltage output will be less than about 25 volts (the transformer is 18 rms volts). The most current you should draw is 0.6 A. (Note the power suply transformer has a power rating of 10 VA.). Calculate the value and power rating of the smallest load resistor you can use. (30 ohm 10w) Vary the load resistor and read the current, the DC voltage across the load (with a DMM or one channel of a DC connected oscilloscope), and the ripple across the load (use an AC coupled oscilloscope.) Plot these two measurements (voltage on the left y axis, ripple on right y axis) vs current (on the x axis). This one graph will tell you most of what you want to know about any power supply.

What is the regulation of your power supply? What is the ouput resistance of your power supply? Note that the dynamic resistance can be defined as $\Delta V / \Delta I$.

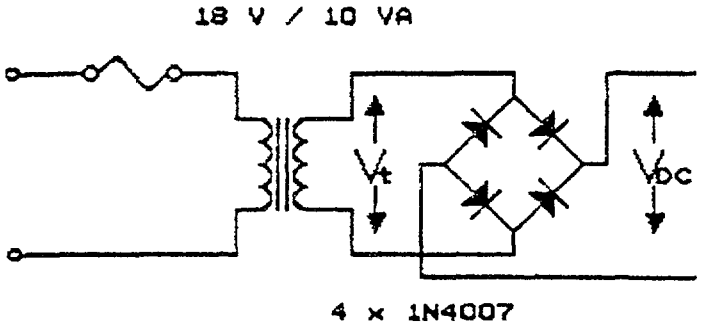


Fig. 1.1.2:

Full-wave bridge rectifier.

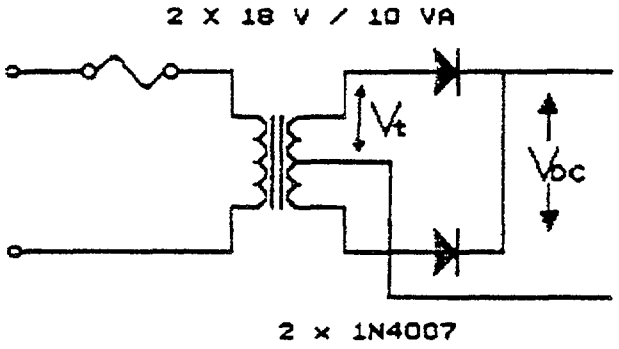


Fig. 1.1.3:

Full-wave center tap rectifier.

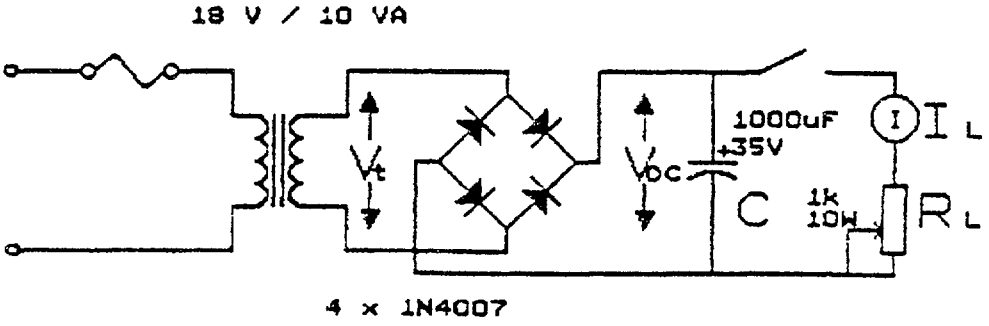


Fig. 1.1.4:

Rectifier circuit with full-wave bridge and filter.

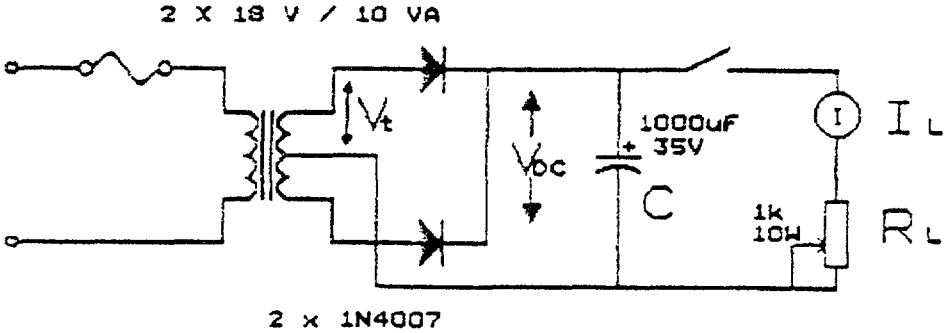


Fig. 1.1.5:

Rectifier circuit with full-wave center tap and filter.

D. Check some theoretical relationships. The maximum votage output from a power supply is given by

$$V_{DC} = 1.41\ V_T - 0.8\ n$$

where V_{DC} is the unloaded voltage, V_T is the rms output of the transformer and n is 1 for a full wave center tap configuration and 2 for a full wave bridge rectifier circuit. (Try to derive this equation. Where do the 1.41 and the 0.8 come from?

A relationship for ripple often used is

$$V_{ripple\ (peak\text{-}to\text{-}peak)} = K\ .\ I_L\ (mA)/C\ (\mu F)$$

where K = 10 (ms) for 50 Hz mains and 8.3 (ms) for 60 Hz mains. How close does your ripple curve come to a straight line and how close does the slope of your line come to the values given above.

E. Select a convienient value of current output, say 200 mA, and change the size of the filter capacitor to a much smaller value (say 1 μF) and to a much larger value (say 10,000 μF). Sketch the traces observed on the oscilloscope and comment on the observations.

EXPERIMENT 1.2

REGULATED POWER SUPPLY USING AN OPERATIONAL AMPLIFIER

OBJECTIVE

This experiment illustrates the action of several common circuits used in a power supply regulator.

REVIEW

This regulator, shown in Fig. 1.2.1, consists of a voltage stabilizing loop and a rather sophisticated foldback current limiting circuit. The current limiting components include Q2, Rs, R3, R4, and R5. The other components are associated with the voltage stabilizing circuit.

The components D1, R1, and C1 provide a filtered, but unregulated, voltage source to power the operational amplifier and the voltage reference source. Because the characteristics of the operational amplifier are independant of its supply voltage, the only requirement is that this voltage be higher than the regulated voltage. The reference voltage is provided by R2 and Z1. Because Z1 is a zener diode, it does not have to be provided with a regulated voltage source. Note that the quality of the regulator is entirely dependant on the quality of Z1. The resistor string, R7, R8, and R9, allows the operational amplifier to sample the regulated voltage. This string can take various forms. The ratios of these resistors determines the range over which the output voltage can be adjusted and the sensitivity of the output voltage to small changes in the adjustment of the trimmer, R7. The pass transistor is controlled by the operational amplifier in such a way as to keep the voltage sampled from this resistor string exactly equal to the reference voltage.

The action of the operational amplifier on the pass transistor can be easily understood by first noting that under normal load conditions, Q2 is cut off and the current limiting circuit is not working. The operational amplifier compares the reference voltge developed across Z1 with the voltage on the resistor string attached to the regulated output. If the output voltage tends to decrease, this sample voltage will decrease, causing the output of the operational amplifier to increase, raising the base voltage of Q1, causing it to conduct

The foldback type current limiter circuit works as follows: under low current conditions, the voltage drop across R_s is less than the voltage developed across R_3 and R_4, which produces a bias at the base emitter junction of Q_2. For that reason Q_2 is cut-off.

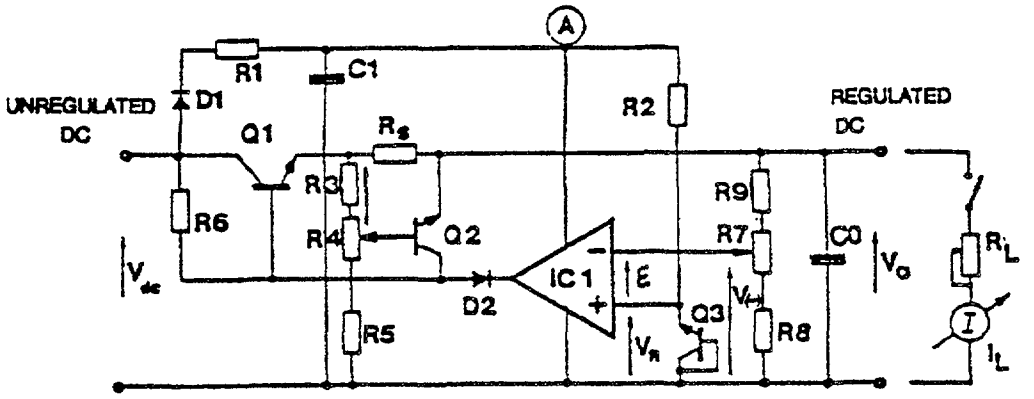


Fig. 1.2.1:

Regulator for power supply using an operational amplifier

Suggested values:

R1 = 180R	Q1 = BD651
R2 = 180R	Q2 = 2N3904
R3 = 830R	Z1 = 6V@,1/4W
R4 = 500R	IC = LF356
R5 = 15K	D1 = 1N4007
R6 = 10K	D2 = 1N4148
R7 = 1K	C1 = 100/35V
R8 = 2K2	C0 = 10/25V
R9 = 1K	
RS = 5R6/1W	
RL = 1K/10W	

The moment at which Q2 starts conducting is when:

$$I_{max.}\ R_s = k\ V_o + 0.5\ V \qquad \text{(Eq.1.2.1)}$$

where k is the fraction of output voltage developed across R_3 and the upper part of R_4 (k is actually adjusted with R_4).

As Q_2 starts to conduct, it takes the current which previously went through the base of Q_1; thus reducing the amount of current Q_1 can pass. The output current cannot be greater than $I_{max.}$

When there is a short circuit at the output terminal,s the output voltage V_o equals zero. Because the base current of Q_2 is negligible, it is easy to conclude that

$$I_{Sc}\ R_S = 0.7V \qquad \text{(Eq.1.2.2)}$$

It can be noted that the short circuit current I_{Sc}, is smaller than the maximum current I_M. Also note that the regulated voltage is sampled after R_S so that R_S does not add to the output impedance of the regulator.

The experiment permits the testing of the circuit, verifying the actions explained above.

EXPERIMENT

With properly selected values for the components, a 6-14V/25mA regulated power supply can be assembled.

Use the circuit assembled in Experiment 1.2 of this series of experiments to provide unregulated DC to the regulator shown in Fig. 1.2.1.

A. Adjust R_7 to obtain 10V as the output voltage V_O.

Measure

V_O =

V_R = depends on the characteristics of Z1

$V_{(-)}$ =

V_A = should be equal to the peak value of Vdc

V_B = V_O + 0.6V (at no load)

B. Reduce the value of C until there is an observable ripple at the input V_{dc}. Measure the ripple at the output.

(1) $V_{\text{ripple at input}}$ =

(2) $V_{\text{ripple at output}}$ =

$$\textit{ripple rejection} = \frac{(1)}{(2)} =$$

C. Change the mains voltage using an autotransformer and observe the output voltage variation ΔV_O = . Calculate the regulation against mains variation.

D. Change the load so that the current goes from I_L = 0 to full load, and observe the output voltage variation V_O. Calculate the regulation against load variation.

E. Adjust R_4 to obtain 1V at V_F. Progressively increase the load current monitoring the output voltage up to the point when V_O starts to decrease. At this point measure:

V_{RS} =

V_{BEQ2} =

$k V_O \approx V_F$ =

Record I_M and verify equation (Eq. 1.2.1).

F. Short circuit the output, measuring I_{SC}. Verify equation (Eq. 1.2.2).

G. Plot the V-I characteristic of the regulator. Draw progresivelly more current from the power supply, by reducing the load resistor from a high value to a low, plotting I on the x-axis and V_O on the y-axis. Determine the output resistance, R_O, from your graph. Plot R_O versus current.

Notes:

EXPERIMENT 1.3

AUXILIARY POWER SUPPLY ± 15V/100mA

This experiment demonstrates the properties of a three terminal voltage regulator.

OBJECTIVE

A three terminal regulator is an integrated circuit which includes, in one simple package, all of the circuits necessary to provide a constant voltage from a unregulated power supply. In this experiment two of these regulators will be used to construct a dual voltage regulated power supply, of a type often used to power operational amplifiers. Operational amplifiers typically require bipolar power supplies, hence both a positive and a negative voltage must be regulated. The simple power supplies described here are intended to be used as a building block for any application requiring +15 and -15V at 100 mA, typically when operational amplifiers are used.

REVIEW

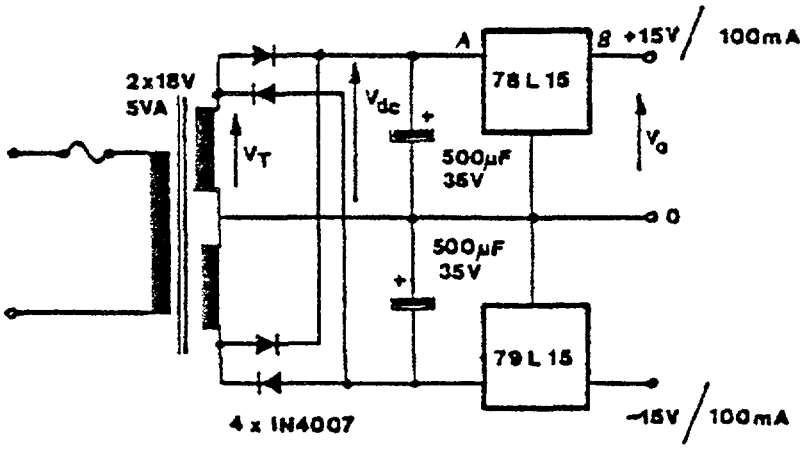


Fig. 1.3.1: Rectifier circuits with full-wave center tap.

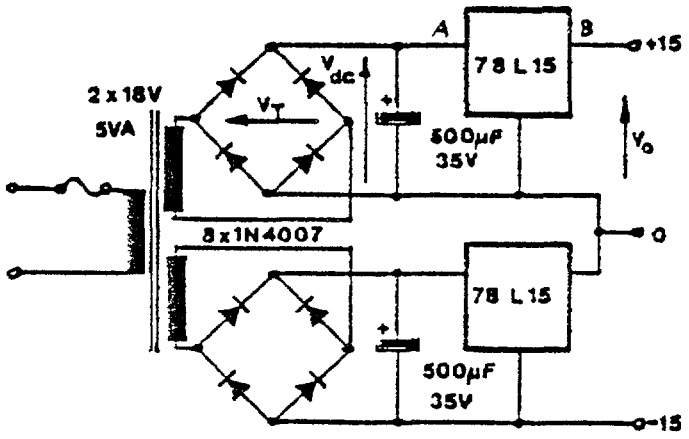


Fig. 1.3.2: Rectifier circuits with full-wave bridge.

Two possible versions can be assembled. Version (a) uses four rectifier diodes and two complementary three terminal regulators, a 78L15 for the positive voltage and a 79L15 for the negative voltage.

The (b) version uses only one type of monolithic regulator, a 78L15, at the expense of using two bridge rectifiers (or eight diodes).

In either case the basic relations between AC and DC voltages, ripple rejection, and regulation capability of the power supply will be examined.

EXPERIMENT

Assemble one of the two possible versions. Take the following measurements. You must calculate the value of the load resistance necessary to draw the 100 mA. Be sure that resistor used has enough power dissipation capability.

A. Measure the following parameters at no load and full load conditions:

	V_T	V_{dcc}	V_o	V ripple at A	V ripple at B
$I_L = 0$					
I_L = 100 mA					

Discuss and comment on these results.

B. Calculate the regulation against load variations. (Take the values obtained from A). Compare with the value given in the data sheet.

$$\%regulation = 100 \times \frac{V_{(full-load)} - V_{(no-load)}}{V_{(no-load)}}$$

C. Calculate the ripple rejection factor at full load:

ripple rejection = (V ripple at A) / (V ripple at B)

This ratio usually appears in data sheets in units of dB. Compare your measured rejection with that given in data sheets. Note that

ripple rejection (dB) = 20 log (V_{rA} / V_{rB}).

D. Short circuit the output. Measure the short circuit current, I_{sc}. Do not try to make this measurement on any power supply which does not incorporate short circuit protection.

EXPERIMENT 1.4

REGULATED POWER SUPPLY USING A MONOLITHIC VOLTAGE REGULATOR

OBJECTIVE

This experiment illustrates the utilization of a monolithic regulator in which the reference, the error amplifier, and the current limiter are all included in the same package.

REVIEW

The LM 723 is a versatile monolithic voltage regulator used in this experiment to build a 5V/1A power supply mounted on a Eurocard board.

As the LM723 supplies only 150 mA, an external pass transistor is used to increase the regulated current capability.

For details concerning the operation of the regulator itself, read the corresponding data sheets. As shown in Fig. 1.4.2, this experiment uses an auxilliary power supply (consisting of a voltage doubler D_1, C_2, D_2, C_3, R_1 and D_3) to provide power for the LM 723. Resistors R_4, P_2 and R_3 fix the maximum and short circuit current as they make, together with the internal current limiting transistor, a fold back current limiter. Resistors R_6, P_1 and R_7 fix the output voltage.

Note that separate wires are used to sense the output voltage. This technique is used in those cases where the load is far from the power supply and the voltage drop in the cables is to be compensated. Figures 1.4.1. and 1.4.2 illustrate this situation. In Fig. 1.4.1 we have the situation with local sensing, at the output terminals. The voltage drop is not compensated, the load receives a lower voltage.

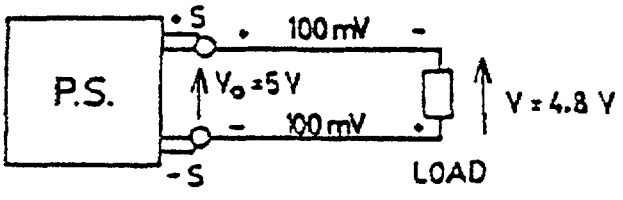


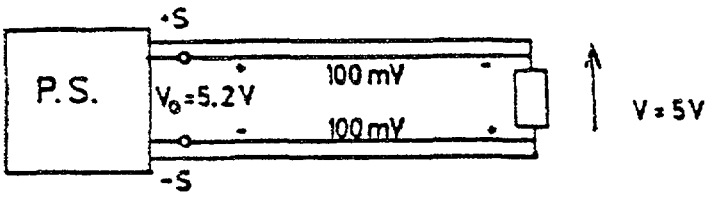
Fig. 1.4.1:

Local sensing at the output terminals.

Fig. 1.4.2 shows the circuit in the case when the sensing is done at the load position through non-current carrying cables so that the full voltage is developed there. The drop in the current-carrying cables makes the voltage at the output terminals 5.2 v.

Fig. 1.4.2:

Remote sensing at the load terminals.



EXPERIMENT

The circuit diagram of the regulated power supply is given in Fig.1.4.3 . The components layout is in Fig. 1.4.4.

In order to be sure that the construction of the circuit is proceeding properly, the assembly is done in steps.

A. Connect the transformer, using the 11V tap on the secondary for 220V and the 10V tap for 240V line voltage. Mount rectifier bridge, diodes D_1, D_2, and D_3, capacitors C_1 to C_4, and resistor R_1.

Measure the voltage across C_3 and D_3. Make sure they are the expected values.

B. Mount the rest of the components. At the output terminals, connect the sense lines with jumpers to the output lines.

Increase progressively the line voltage, using the variable autotransformer, to the nominal value. Adjust P_1 to get +5V at the output terminals.

Measure the following parameters:

- line regulation
- load regulation
- ripple rejection

Follow the instructions given in Experiment 1.3 of this series.

C. Adjust the load resistor to draw a current of 1A. Adjust P_2 to start the current limiting action.

Short circuit the output and measure the short circuit current, I_{sc}.

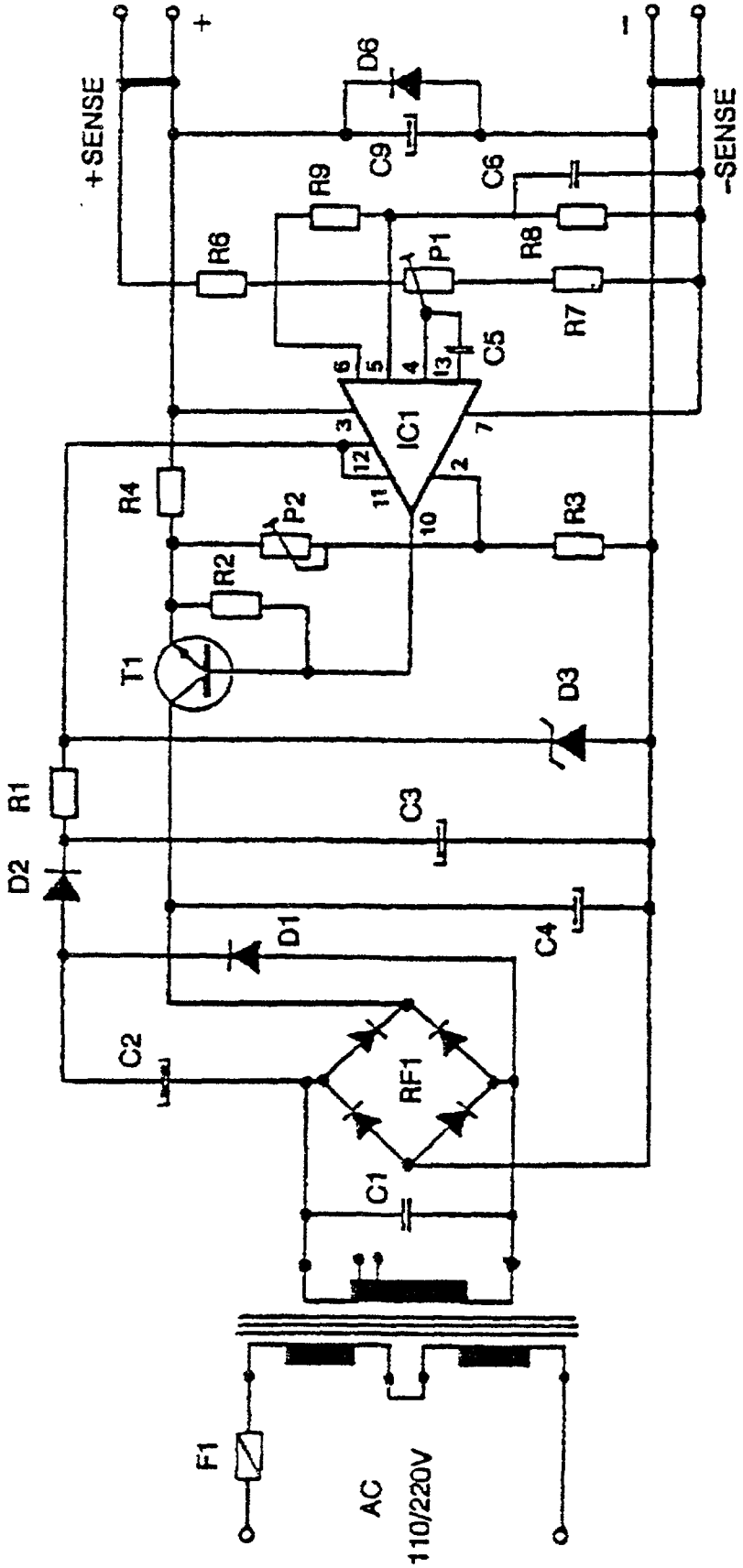
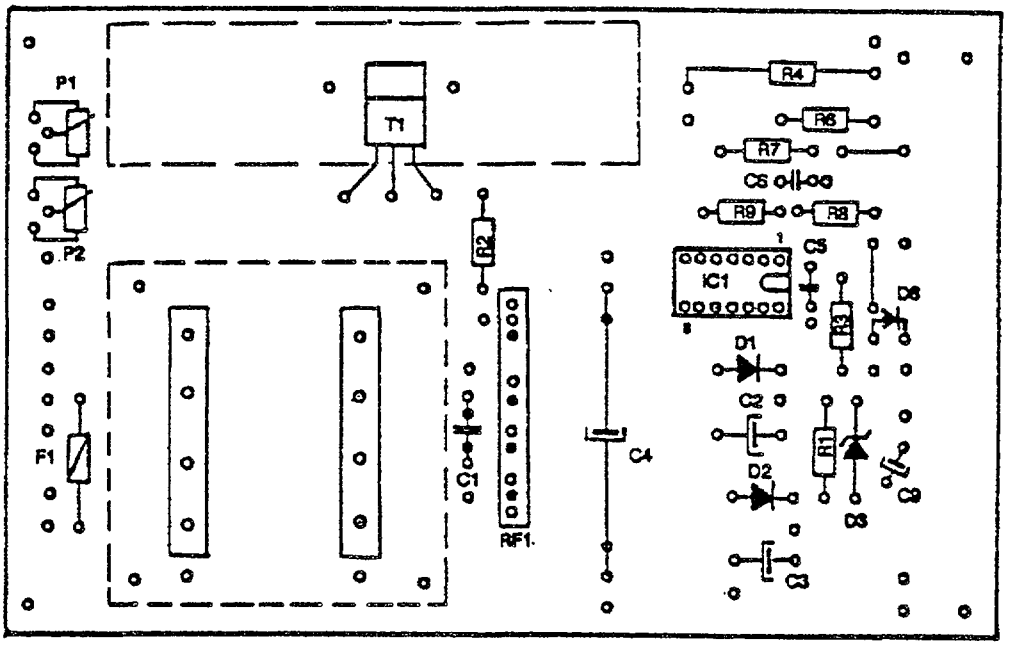


Fig. 1.4.3:

Regulated power supply with monolithic regulator.

Fig. 1.4.4:

Components layout for Experiment 1.4.



Suggested values for the requested power supply:

Transformer	pr. 110/220V, 50/60 HZ	
RFI	full wave rectifier	1,5A/20 VAC (B 80 C 37000/2200)
IC 1	integrated circuit	LM 723 CN with socket
T 1	Darlington power transistor NPN (BD 651)	
D 1, 2, 6	silicon diodes	60V/1 A (1N4004)
D 3	zener diode	12V 1 W (BZX 85 C 12)
C 1	capacitor	0.1 μF/100V
C 2, 3	capacitor, electrolytic	47 μF/40V
C 4	capacitor, electrolutic	2200 μF/15V
C 5	capacitor, ceramic	470 p
C 6	capacitor	2.2 μF/25V
C 9	capacitor, electrolytic	100 μF/25V
P 1, 2	trim potentiometer	500 R
R 1	resistor , metal film	511 R
R 2, 3	resistor, metal film	3 K
R 4	resistor, wirewound	1R2, 5W
R 6	resistor, metal film	1 K
R 7, 8, 9	resistor. metal film	3 K

Suggested values for the overvoltage protection circuit

T2	transistor	PNP (2N3906)
D4	Zener diode	5.1 V, 0.5 W
D 5	thyrisor	4A/100V (2N4441)
C 7, 8	capacitor	0,1 μF/ 100V
P 3	trim potentiometer	500 K
R 10	resistor	1,5 K
R 11	resistor	1 K
R 12, 13, 14	resistor	100 R

Mount on a separate board the overvoltage protection circuit illustrated in Fig. 1.4.5. Should the output voltage reach the (adjustable) threshold, the circuit triggers and short circuits the output, thus driving the power supply into current limiting or blowing the fuse in case the pass transistor is short-circuited. In both cases the load is protected against overvoltages.

Measure the trigger level of the protection circuit by increasing the output voltage with potentiometer P_1.

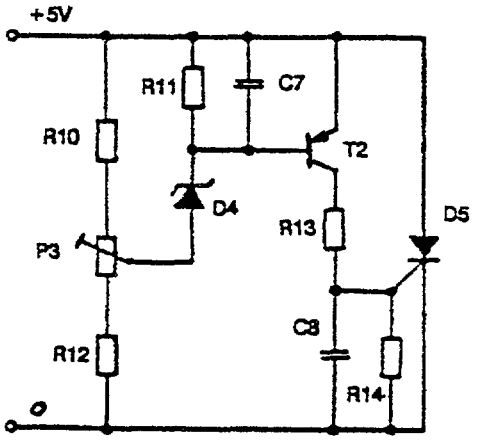


Fig. 1.4.5: Overvoltage protection circuit

Comments on exercise 1.4

A much simpler overvoltage protection circuit is shown in Fig. 1.4.5.

The advantage of this circuit is that fewer components are required. A disadvantage is that the trip voltage is not adjustable.

It is important to know where to connect such a protection circuit and the associated fuse. The block diagram in Fig. 1.4.6 should clarify the situation.

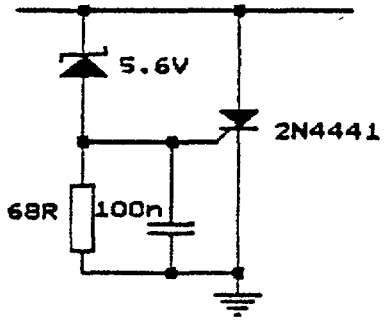


Fig. 1.4.6: Simple overvoltage protection circuit.

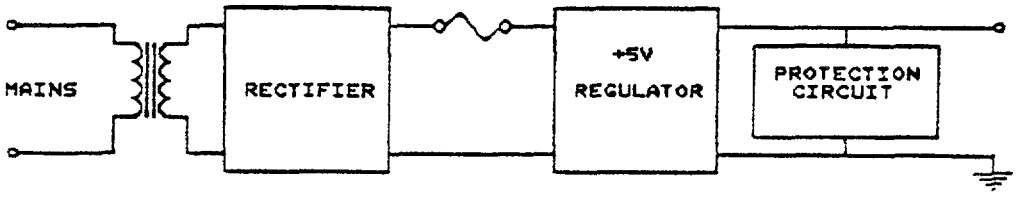


Fig. 1.4.7: Position of protection circuit in a regulated power supply.

Notes:

EXPERIMENT 1.5

HIGH VOLTAGE POWER SUPPLY

OBJECTIVE

This experiment permits the analysis of a typical circuit used to supply high voltage to a detector.

REVIEW

The power supply to be assembled and tested produces 900V at approximately 1 mA. The circuit is shown in Fig. 1.5.1. It is instructive to analyze in some detail the blocks which make up this circuit. As the individual blocks are described in the text below, draw boxes around the appropriate parts of the circuit diagram, and label them for future reference.
A square wave oscillator feeds a driver stage which is connected to a step-up transformer. The center tap of the primary winding is connected to a 12 V supply coming from a voltage regulator. Under these circumstances, a 440 V square wave is developed in the secondary winding.
This AC voltage is rectified in a doubler type rectifier circuit.

The doubler circuit works as follows: diode D_1 charges capacitor C_1 to the peak of the voltage present at the secondary. Between A and B a voltage which is the sum of the DC voltage developed at C_1 plus the AC voltage at the secondary winding is in turn rectified by D_2 and filtered by C_2. The result is that capacitor C_2 is charged to the peak value of the voltage existing between A and B, that is to say, twice the peak voltage at the secondary winding.

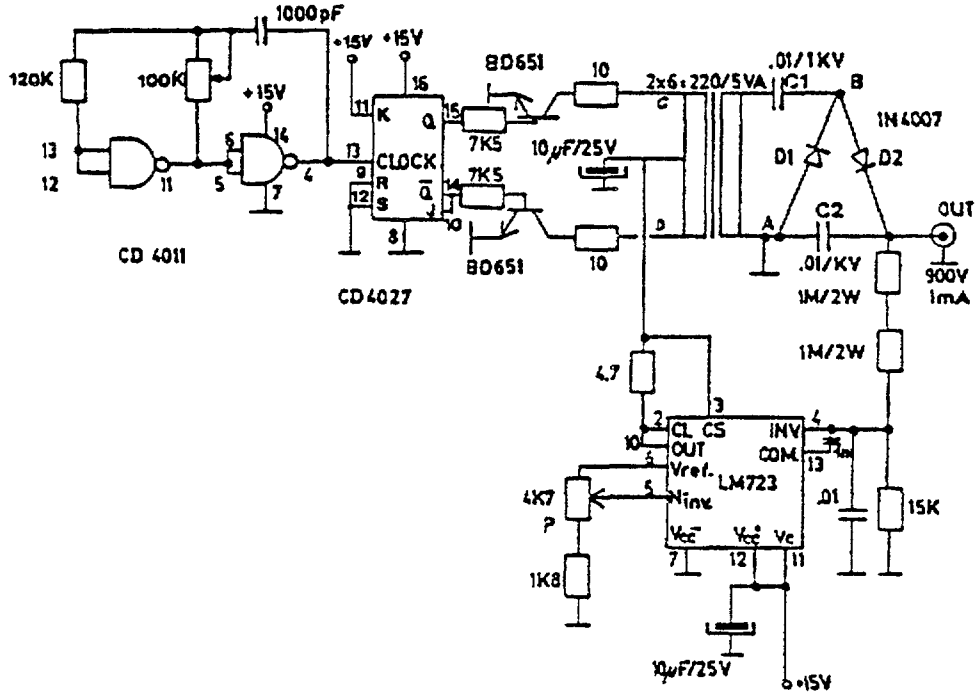


Fig. 1.5.1:

High voltage power supply

The voltage regulator samples the high voltage and adjusts the potential of the center tap to compensate for possible variations of the high voltage. Potentiometer P permits the final adjustment of the high voltage.

A square wave oscillator generates the initial signal. The oscillator is implemented with a CMOS integrated circuit. A flip-flop assures a perfectly symmetrical wave at the primary winding of the transformer, avoiding possible circulation of dc current through it.

Note that this is an experimental power supply, build to illustrate the principles upon which a commercial unit is built. For a practical application, additional circuits are needed such as filtering networks, high voltage potentiometer for adjustment of the output voltage, provision for inverting polarity, and provision for output current measurement.

> BE CAREFUL WITH THE HIGH VOLTAGE OUTPUT. If the oscilloscope probe you are using is not rated for 1.500 V, put a resistor of 10 M in series with the tip.

EXPERIMENT

A. Assemble the circuit as is indicated in the circuit diagram, Fig. 1.5.1. Connect an external 15 V power supply and check the following:

- that the oscillator is running. Measure the frequency of the oscillator. f_{osc} =
- that there is a symmetrical square wave at the flip flop output

- that the collector of the driver transistors reaches saturation level. V_{sat} =
- that there is high voltage at the output. V_0 = . Adjust P if necessary.

B. Measure the voltage across the filtering capacitors. V_{C1} = and V_{C2} = Reduce the output voltage by adjusting P and observe the wave forms at D and at C. Sketch them.

Connect a suitable load, (calculate it) and measure the ripple.

While connecting a load, measure the centre tap voltage. Does it change? Why? Did your waveforms change?

C. (Optional). Add one more multiplying stage. Consult your instructor before applying power so that your circuit can be checked for possible overload of components. Measure the output voltage.

Connect an external generator to the clock input of the flip-flop. Try to find an optimum frequency for which the current drawn from the voltage regulator is a minimum.

Experiment 1.6

DC-DC CONVERTERS

OBJECTIVE

The purpose of this experiment is to provide experience with the modern technique of DC power transfer from one voltage level to another.

REVIEW

It is easy to change the level of an AC voltage with a transformer, but more difficult to change a DC voltage. Often nuclear instruments require small amounts of DC at various voltages, as for example, high voltage to power a detector. These voltages can be provided by a DC to DC converter. Basically, one needs a oscillator to interupt a DC signal, a transformer or energy storing inductor to change the voltage level, and an ordinary rectifier and filter to reconvert the signal to DC. The oscillator is often operated at high frequency so that the transformer can be small and light.

Other types of voltage regulators, called switching regulators, have been developed to take advantage of the space and weight savings at the expense of considerable complications in the circuitry.

Three different types of operation will be studied here:

- a push-pull mode converter,
- a single transistor forward converter, and
- a flyback or blocking converter.

In the past, the DC-DC converters in nuclear electronics have been mostly used to supply the detector high voltage; now they often appear in the low power supplies and in switching regulators.

A typical DC-DC converter consists mainly of four parts:

a. the oscillator or control circuitry

b. the driver stage

c. a transformer or energy storage inductor

d. rectifier and filters.

The first part includes an oscillator, a potentiometer to control pulse width and circuitry to provide regulation. The driver stage is necessary to switch the high current required

to provide appreciable power. The transformer or energy storage inductor actually changes the voltage. The last part performs conventional rectification and filtering.

Preliminary experiment (assembling and testing the controlling circuitry)

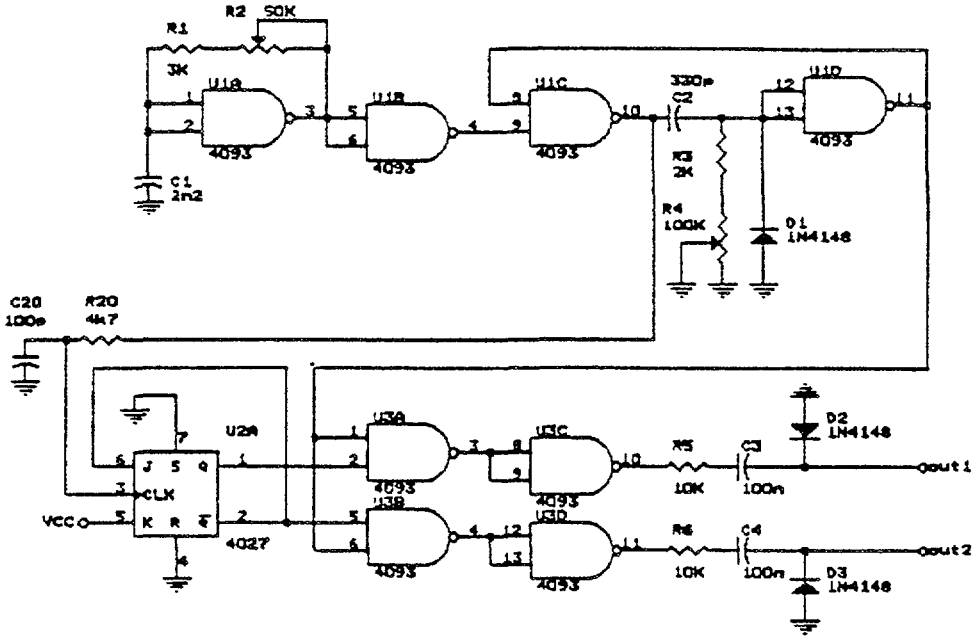
EXPERIMENT

Assemble the controlling circuitry of these experiments as shown in Fig.1.6.1. Apply 12V to the circuit and adjust the current limitation to 150mA so that later, when you test the complete converter, the driver transistors will be protected from possible burn out. Test this circuit and compare the waveforms shown in Fig. 1.6.2 with your results.

Next, wind a transformer coil with 4 windings (2 x 24 turns and 2 x 12 turns).
Note: The start and end of the coils should not be connected together to provide flexibility in using these windings in the different modes of a DC-DC converter (see Fig. 1.6.3).
Experiment 1 (Push-Pull Converter)

Fig. 1.6.1:

Control circuit of DC-DC converter



Build a push-pull converter by connecting the control circuit of Fig. 1.6.1 to the power stage of Fig. 1.6.4. The design of a good DC-DC converter is difficult. The frequency, the ratio of on time (T_{on}) to the period (T), and the inductance have an important effect on the efficiency of the circuit. Furthermore, they all interact with each other. Here we can readily adjust the frequency (f), with R2, and the T_{on}/T ratio, with R4. It is easy to measure the output voltage (V) and the current in the primary of the transformer (with an oscilloscope across R3). Select a reasonable load (drawing about 50mA). Plot V (on the x-axis) versus f (in the y-axis) for T_{on}/T = 0.5. Next, plot V versus Ton/T with f set at the value which gave the maximum volatge in the previous part. Skech some of the waveforms observed across R3. If you have time, adjust both the ratio T_{on}/T and f, to maximize V. Repeat the experiment for different loads.

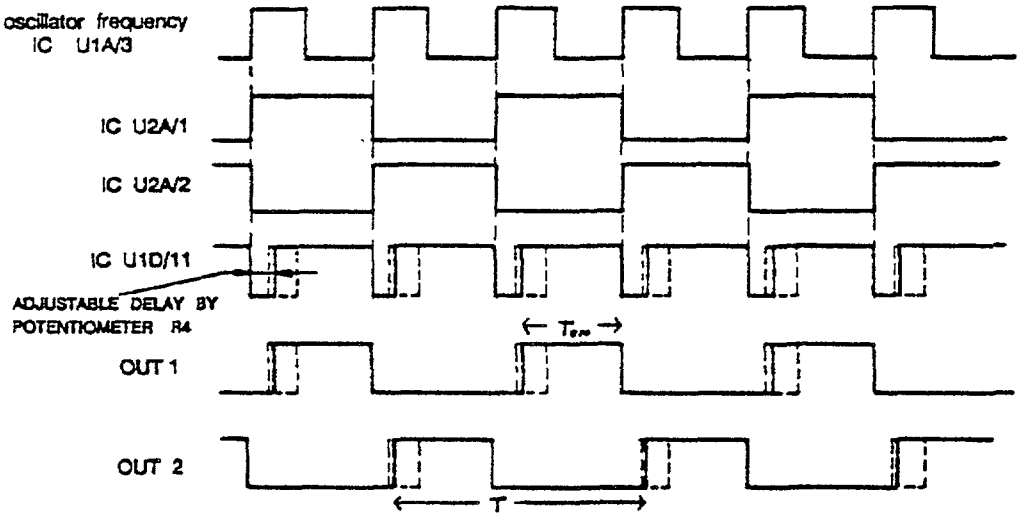


Fig. 1.6.2:

Waveforms of Controll circuit

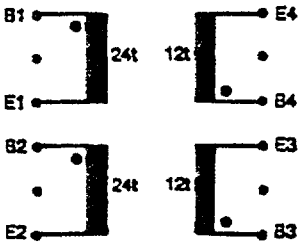


Fig. 1.6.3:

Transformer coil pin configuration.

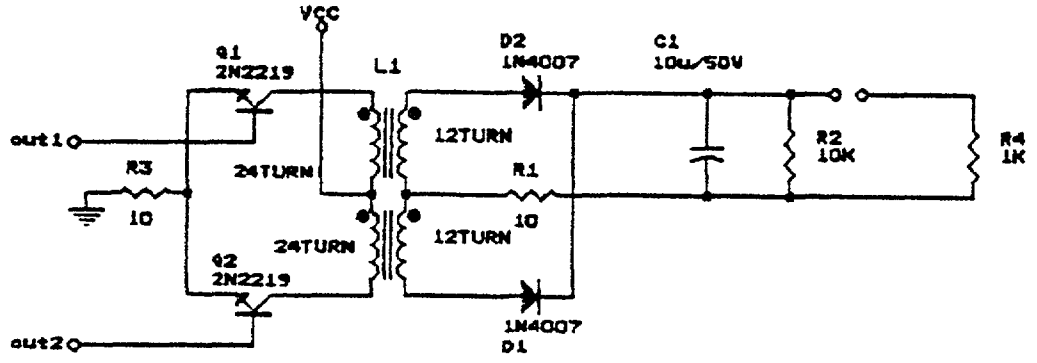


Fig. 1.6.4:

Power stage of push -pull converter

Experiment 2 (single forward coverter)

Change your converter to the form shown in Fig. 1.6.5. Repeat the measurements suggested in the previous part, using diode D5. Repeat the experiment using diode D6, noting the effect of the faster diode.

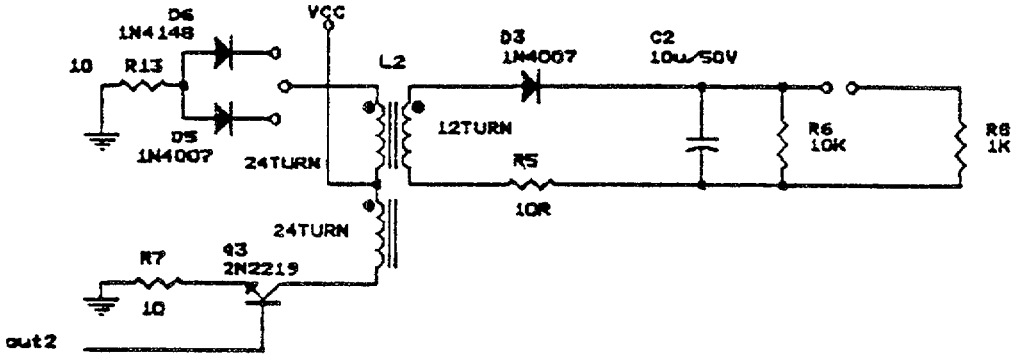


Fig. 1.6.5:

Power stage of a single forward converter.

Experiment 3 (blocking converter)

Change your converter to the form shown in Fig. 1.6.6. Repeat the measurements suggested in the first experiment.

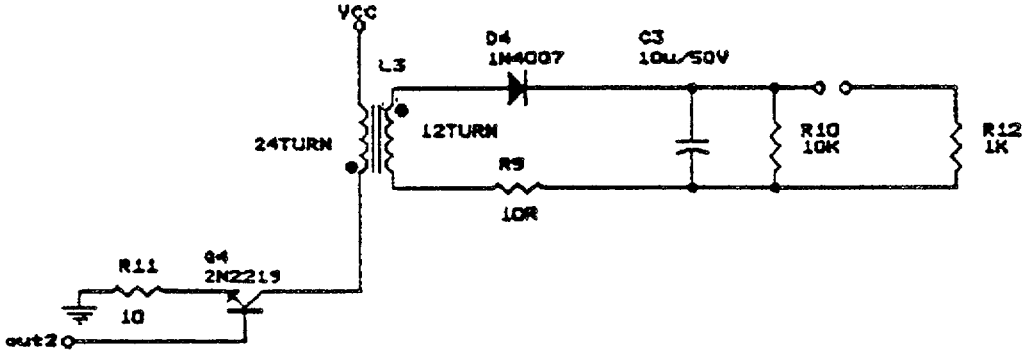


Fig. 1.6.6:

Power stage of blocking converter.

Experiment 4

Try to redesign any of the circuits to get a negative voltage.

EXPERIMENT 1.7

CONSTANT CURRENT SOURCE

OBJECTIVE

In this experiment you will learn how a high precision constant current source can be constructed and how this current can be switched to different points of a circuit. Also an example of logic level shifting is demonstrated.

REVIEW

High precision constant current sources are very important as, for example, in Wilkinson-type ADCs. As we know, in this case the time it takes to completely discharge a capacitor with a constant current has to be measured.

Fig. 1.7.1 shows a constant currect source. In this case, it is really a sink because the current goes from ground to -15 V.

The operation of the circuit is straight forward. The resistor connected to ground supplies enough current to firmly establish the zener voltage which fixes the base voltage of the transistor. The emitter resistor then controls the current thorough the transistor. That current must pass through whatever is connected to the collector. If too much current tends to flow into the transistor, the voltage on the emitter end of the resistor will rise, tending to cut off the transistor with its fixed base voltage. If too little current tends to flow through the transistor, the voltage on the emitter end of the resistor will fall, tending to increase the collector current of the transistor with its fixed base voltage.

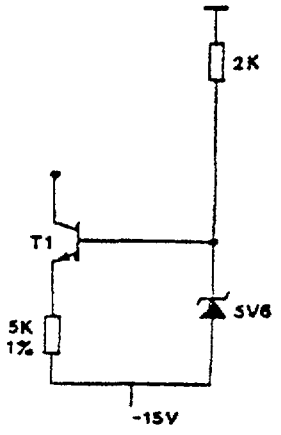


Fig. 1.7.1: Constant current source

Note that the value of the constant current depends mainly on the value of the emitter resistor and the zener voltage. (Develop a formula for the relation!) Three factors effect the value and stability of the current; the zener voltage, the value of the emitter resistor, and the base emitter voltage of the transistor. As long as these items are known and independent of temperature and other influences, one will have a constant current flowing into the circuit.

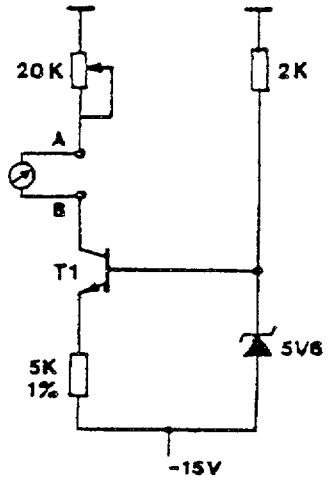
However, these items do change. A look at the wiring diagram of several ADCs will provide examples of more sophisticated tricks used to increase the stability of the constant current circuits.

EXPERIMENT

Construct the constant current source shown in Fig. 1.7.2. Use the ready-made printed circuit board. You will notice that part of this board will remain unused. During the experiment, some features will be added. This circuit is the same as in Fig.1.7.1, with the addition of a meter to measure the current, and a variable 20K resistor to use as a load.

Fig. 1.7.2:

Constant current test circuit.



Vary the load from 0 to 20K. Plot current (on the x-axis) versus resistance (on y-axis) in order to get some idea of the quality of your constant current source. Note that there are some limitations. To get a better idea of the source of these limitations, plot on the previous graph the voltage drop across the load resistor (on the right y-axis). Comment on this graph. What is the effective impedance of your current source? If you have time, make a similar but much smaller current source, and repeat the above measurements.

Current switching

In many applications, as for instance in the Wilkinson ADC, it is necessary to have the current applied at once, with its full constant value, without any turnon delay from T_1. This is only possible if that current is already flowing in another branch of the circuit, and is suddenly switched over to that part of the circuit where it is needed, for instance, to the capacitor to be discharged.

Illustrate one method of switching by completing the circuit in Fig. 1.7.3. When you remove the meter, the 20K potentiometer is disconnected from the collector of T1. Do not install R yet.

This circuit has some resemblance to the non-saturated ECL logic family. These are extremely fast logic circuits which are used only in large mainframe computers and therefore are not included in this manual. We can calculate the voltage level at the base of T2 and T3. Ignoring the small base currents, we find -7.5V for the base of T2 and -8.2V for the base of T3. Since both emitters are connected, it is clear that T2 is conducting, the common emitter voltage is -8.1V, and T3 is cut off.

This can be checked since the 1mA which is "wanted" by T1 will flow only through T2, causing a voltage drop in the 3.3K collector resistor. At the collector of T2 one should measure -3.3V while at the collector of T3 one should find 0V.

Calculate the value of R so that, when it is soldered between the base of T3 and +5V, one will find a voltage of -6.8V at the base of T3. After soldering it, check that T3 is now conducting. The voltage at the common emitter is -7.4V, and T2 is cut off.

The circuit has now been checked statically; and one can see that it is possible to switch the current that is constantly flowing through T1, from T2 to T3 and back. In the case of the Wilkinson ADC, the collector of T3 will be connected directly to the capacitor in the pulse stretcher that has to be discharged.

The next section will help you to test the circuit dynamically.

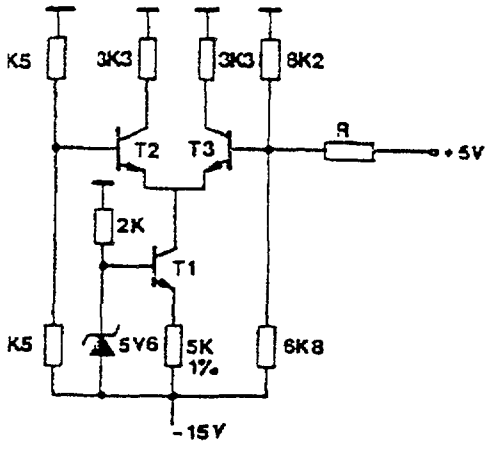


Fig. 1.7.3: Current switching.

Logic level shifting

Instead of connecting the resistor to +5V, add the circuit shown in Fig. 1.7.4.

The switching of the current is normally done under control of logic circuits that are powered from a +5V supply. This method requires a level shifter. Construct the circuit shown in Fig.1.7.4.

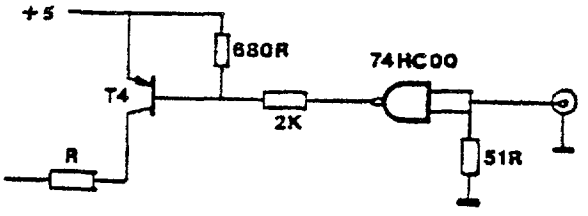


Fig. 1.7.4: Logic level shifting

When a pulse coming from a generator connected to the input is at logic level 0, the output of the NAND gate is high, and T4 is cut off. This means that R is not conducting any current and in that case we know that T2 is ON. When the input pulse is at logic level 1, T4 will go in saturation; and, just like in Fig.1.7.2, one side of R will be at nearly +5V. T3 will conduct the current of 1 mA from T1. Check all this with a fast double trace oscilloscope. Change the frequency of the incoming pulse train, and see how high one can go with this kind of circuit.

(Optional) This simple circuit has been subtly designed. What is the specific function of each of the resistors, and why were their particular values selected? How could they vary from the values given?

Notes:

Experiment 1.8

LINE CONDITIONERS

OBJECTIVE

This experiment will review some basic power line information and provide an introduction to power line conditioners and uninterruptable power supplies.

REVIEW

The typical laboratory provides 220 Vrms (110 VAC) to the experimental area. This voltage is provided from a low impedance source and is DANGEROUS. Treat it with respect.

There are a bewildering variety of plugs used around the world, but most of them support a line cord with three wires. One of these wires is the hot wire and supplies the power to the equipment. Another wire is the neutral wire. It is at ground potential and provides the return path for the current. The third wire is the ground wire. That wire is a safety feature and should be physically connected to the earth at the place where the power enters the building.

Power conditioners are more or less complicated pieces of equipment designed to ensure that only power with the desired voltage and frequency characteristics enter the laboratory. They often contain clippers to remove spikes, low pass filters to remove high frequency noise, and sometimes means to adjust the voltage to meet the usual specifications.

Uninterruptable power supplies (UPS), in addition to the above features, will contain a source of energy (usually batteries) which is used in place of the line voltage in case of a mains interruption.

EXPERIMENT

Figure 1.8.1 shows a typical power receptacle. Often the ground pin will be replaced by a contact on the side. Sometimes the wiring is such that the power pins are reversed. With a voltmeter, locate the hot and neutral pins on your socket and record the voltage measured. Carefully investigate the signal at the hot pin. (Connect the ground side of the probe to the neutral line.) Sketch carefully the waveform observed. Often there are high frequency signals on the line. These signals can be seen by increasing the gain and the sweep speed of the oscilloscope. Sometimes a high pass filter as in Fig. 1.8.2 is useful.

B. A signal conditioner will remove spikes and noise signals from the power line. It will also often help keep the voltage within the limits which

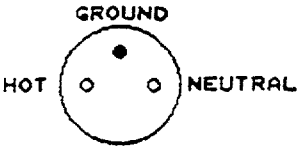
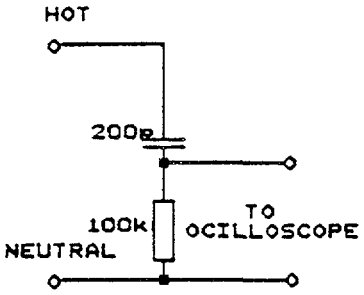


Fig. 1.8.1: Typical power receptacle.

nuclear instruments require. Read the instruction manual for the power conditioner which has been supplied to you. Plug a variable transformer into the power line and plug the power conditioner into the transformer. Again look carefully at the output of the power conditioner with the oscilloscope. Are there any waveform changes? (Use the dual channel feature and superimpose the signal obtained from before and after the power conditioner.) Does a small load, such as a 10 or 20 watt light bulb, affect the waveform? Is any noise still there? Set the variable transformer to give the voltage the power company would like to supply. Plug in the power conditioner and vary the line voltage as mush as possible. Plot the output of the power conditioner (on the y axis) against the input (on the x axis).

Fig. 1.8.2:

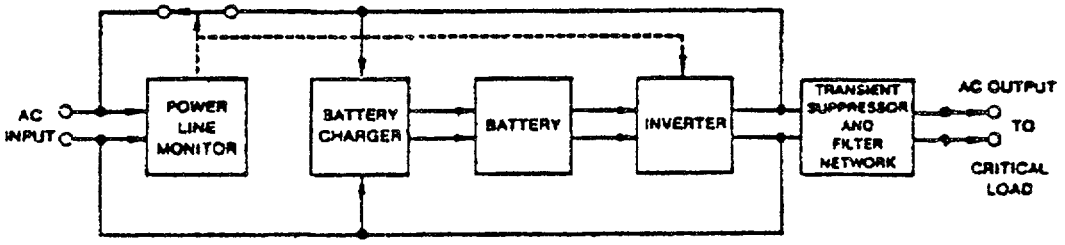
High pass filter used to investigate line signals.



C. An Uninterruptable Power Supply (UPS) usually contains a power source (batteries), control circuits, and conditioning circuits. Read the instruction manual of the UPS which has been supplied to you. A block diagram of your unit is given in Fig. 1.8.3. Plug a variable transformer into the power line and plug the UPS into the transformer. Again look carefully at the output of the UPS with the oscilloscope. Are there any waveform changes? (Use the dual channel feature and superimpose the input and output signals.) Does a small load affect the waveform? Is any noise still there? Vary the input voltage with the variable transformer. Plot the output of the UPS (on the y axis) against the input (on the x axes).

Fig. 1.8.3:

Block diagram of a typical UPS.



Experiment 1.9

SWITCHING REGULATOR

This experiment explains the basic principles behind a switching regulator and provides experience with the parameters that influence the output.

OBJECTIVE

Switching voltage regulators are widely used because of their high efficiency, usually 80% or more, lower price and smaller size compared to linear voltage regulators. Disadvantages include higher noise and ripple at the output of the regulator.

REVIEW

Three basic forms of switching regulators exist. These are step down, step up, and inverting. As the names suggest, the output voltage can be lower or higher than the input or even of inverted polarity. All the regulation is done using a switch, an inductor, a capacitor, and a diode together with special circuitry to control the switch.

A step down switching voltage regulator is shown in Fig.1.9.1.

To make the explanation of the action of the circuit easier, assume that the input voltage, V_i, is constant, the output voltage U_o is constant (except for the ripple), and the output current, I_o, is also constant (the load does not change). The capacitor can not supply current without changing its output voltage. Therefore its current must come from the input. Thus the average current through the inductor I_L, must be equal to the output current, I_o.

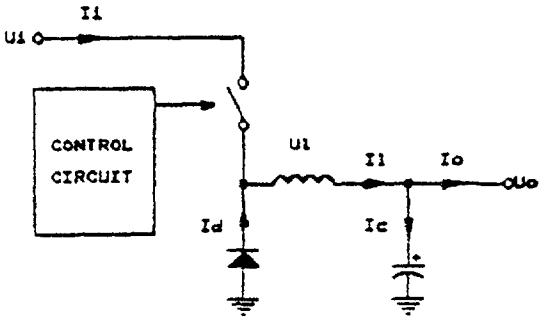


Fig. 1.9.1:

Concept for a step down switching voltage regulator.

Initially assume that the switch is on and the current through the coil equals output current. This condition is shown in Fig.1.9.2, on the following page.

At this moment the voltage across the inductor, U_L is given by $U = U_i - U_o$. By integrating the usual equation for the voltage across an inductor

$$U_L = -L\, dI_L/dt$$

one can show that

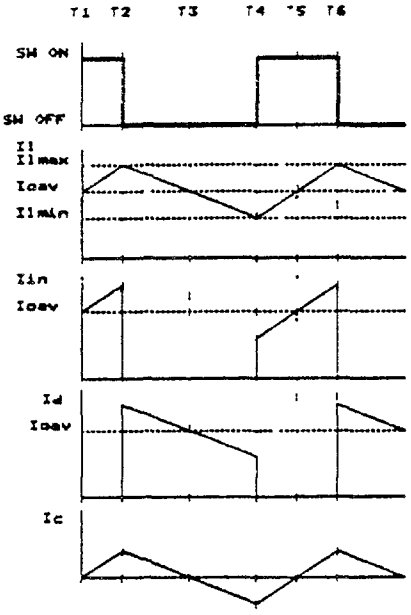


Fig. 1 9.2:

Waveforms in switching power supply.

$I_L = U_L t/L + I_o$.

This shows that if the voltage across the inductor is to remain constant, the current through the inductor must linearly increase with time. This increase lasts as long as the switch shown in Fig.1.9.1 is on. This situation, for step down switching regulators shown in Fig.1.9.2 between the times T_1 and T_2. Immediately after T_1, I_L becomes bigger than the output current Io. The excess flows into the capacitor C.

At T2 the switch is turned off. The current through the coil can not change instantly but neither can it come through the switch. Therefore it starts flowing through diode D. Supposing the voltage drop across the diode to be zero, the voltage accross the inductor at this moment can be expressed as $U_L = - U_o$. This voltage comes from a linear decrease in the current I_L. This decrease can be seen in Fig.1.9.2 between points T2 and T4.

The current I_L is still bigger than Io between T2 and T3, therefore the excess still flows into the capacitor as Ic. After T3, I_L becomes less than Io and the capacitor must supply the difference.

At T4 the switch is turned on again. The voltage across the inductor is again $U_L = UI - U_o$ and the current through the coil increases linearly from the minimal value achieved the moment before T4. During the time from T3 to T5 the current I_L is lower than Io. Therefore the capacitor has to supply the difference of the two.

At T5 the current through the coil becomes equal to the output current. It is still increasing so the capacitor again stores the extra charge. This action continues untill T6, when the switch is turned off again and the action repeats itself from T2.

Charge is stored in the capacitor between T1 and T3 and taken out between T3 and T5. If these two charges are equal, then the average voltage at the output of the regulator will be constant.

If I_o were greater, then the charge stored in the capacitor would be less and the charge taken out more. The result would be less output voltage. To maintain the same voltage at the output, the charging time for the capacitor would have to be increased. By changing the ratio of switch on time to switch off time the voltage can be regulated.

A special circuit is needed to control the switch. Almost any voltage regulator can be used. Special switching power supply control curcuits can be found on the market. These usually monitor the output voltage and adjust the switch on to switch off time as necessary to maintain the voltage constant.

Charging and discharging the capacitor causes a ripple on the output, U_o. The ripple depends on the value of the components used and is usually in the range of a few tens

of a millivolts. The switching frequency is usually above 20KHz and the change in I_l can be as high as 80%.

In a real circuit, the switch is replaced with a transistor. When the transistor is conducting only the saturation voltage exists across it; therefore the power dissipated in it is small. When it is off, no power is dissipated there either. But during the transitions, the power dissipated can be quite high. It is wise, therefore, to select a transistor with switching times as short as possible to decrease heating. The diode must also be fast enough.

EXPERIMENT

The circuit to be constructed is shown in Fig.1.9.3. A three terminal regulator, the LM317, is used as a control circuit. It monitors the output voltage through R3, R4 and R6 as in the usual version. A transistor, a diode, an inductor, and a capacitor are added as described

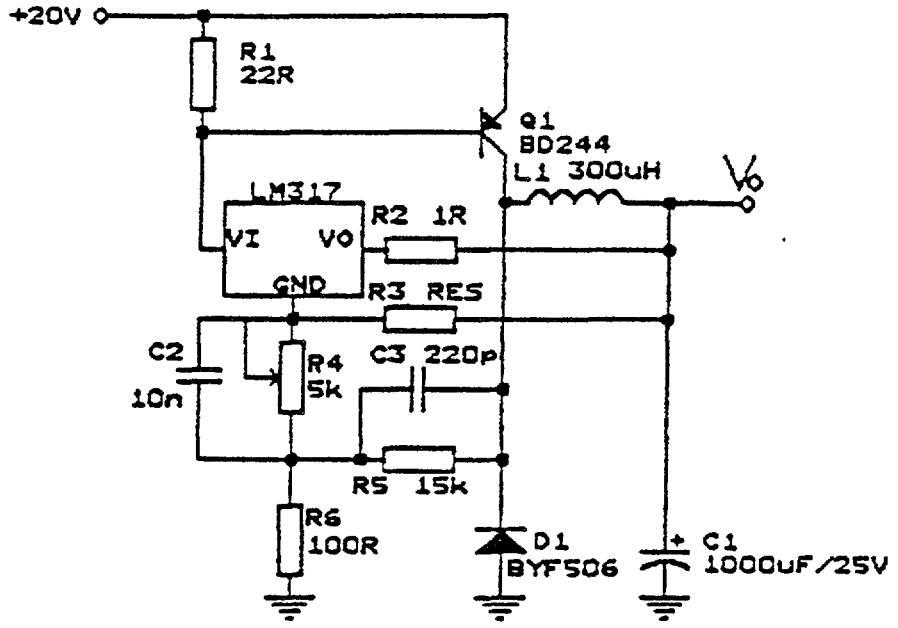


Fig. 1.9.3:

Step down switching regulator.

for the step down regulator. A slightly different way of controlling the switch is employed here. It is turned on for a predefined time (R5, C3) every time the output voltage drops under the value set by R4. When it drops, LM317 draws current through R1 and this turns on the transistor, increasing current through the coil, and filling the capacitor.

The output voltage can be set within the range between 3 and 25 volts by R4. The maximum output current is 0.5A.

Assemble the circuit as proposed and set the output voltage to 5 V. Measure the output voltage, the ripple, and the efficiency (power dissipated in the load/ power entering the circuit) for various values of output current. Use a current up to 500 mA in increments of 100 mA. Graph your results, putting current on the x-axis and the other quantities on the y - axis.

Notes:

PART TWO

ANALOG CIRCUITS

Analog circuits - an introduction.

The response of nuclear detectors to radiation is small charge (10^{-16}–10^{-13} As) delivered within short time interval (1ns–1μs). This charge is deposited on a capacitor of few picofarads, building the voltage of 100 μV to 100 mV. The pulse countrates often exceed 50.000 cps. Pulses arrive at random times. To sense such signals and to bring them to the level where they can be converted to digital signals is the formidable task which can be accomplished only by the most sophisticated analog electronics. The accuracy for the typical non-nuclear analog data processing is around one percent; in nuclear instrumentation more than ten times higher accuracy is required. To achieve this, high quality components should be used, and many design tricks applied.

In the preamplier which is still manufactured from the discrete components, the noise problem must be considered. The amplification of fast signals is not very difficult but the DC coupling through all amplifying chain might introduce large DC shift at the output. How to keep base line at zero is the task of the baseline restoration.
The signal to noise ratio is improved by proper signal filtering, depressing the signals in the frequency domain where the signal contribution is small. The complex pole filters realize the task.

Often only the selected events are worth to be observed. It is also useful to exclude from analysis events which are of no interest, or where erroneous results are expected. The proper selection is achieved by using linear gates.

Analog technique is also useful in time interval measurements if these intervals are converted into pulses with amplitudes proportional to time periods. Then, the normal amplitude analyses of these pulses records time intervals.

How to implement all above task by approariate electronic circuits, is covered by exercises in Part Two.

EXPERIMENT 2.1

DISCRIMINATOR

OBJECTIVE

Studies of the input-output relation for an open loop operational amplifier application are performed to obtain a practical voltage discriminator. The influence of the positive feedback is demonstrated.

REVIEW

The electronic symbol for an operational amplifier is shown in Fig. 2.1.1. Its output voltage is $V_0 = A\,(v^+ + v^-)$, where A is a very large number ($A = 10^5$). With $v^- = 0$, the relation between input V^+ and output V_0 is plotted in Fig. 2.1.2.A.

The output voltage V_0 exhibits a sharp jump in the vicinity of the zero input voltage, and the amplifier output voltage swing is limited by the amplifier operating voltages E^+ and $-E^+$.

Accepting the $-E^+$ voltage as the logical low state and the E^+ voltage as the logical high state, the circuit can tell the polarity of the input voltage applied to the input.

If the voltage V_{ref} instead of the zero voltage is connected to the noninverting input, the input-output relation becomes, for $V_{ref} = 3V$, $v_0 = A\,(V^+ - 3)$, as represented in Fig. 2.1.2.B.

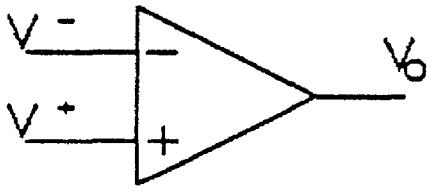
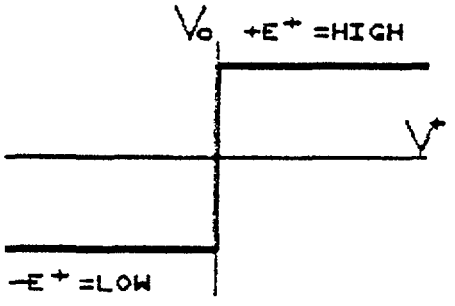


Fig. 2.1.1: Operational Amplifier



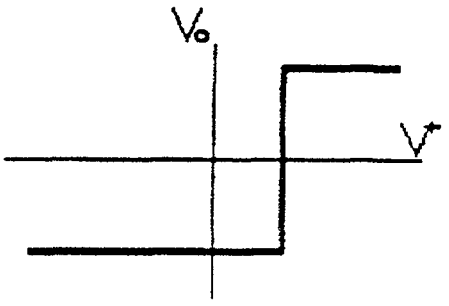


Fig. 2.1.2: Input-output relation for operational amplifier with (A) $V_{ref} = 0\,V$ (B) $V_{ref} = 3V$

The circuit can discriminate between input voltages smaller than V_{ref} and greater than V_{ref}. However, with $v^- = V_{ref}$ the output V_0 might be zero.

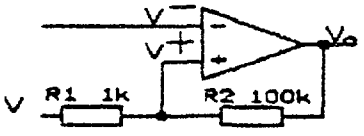
In order t o improve the sensitivity of the system, positive feedback is introduced (Fig. 2.1.3). Previously stable circuit becomes unstable, i.e. only E^+ or $-E^+$ output states are possible. This can be proved as follows. Assume that both input signals v^- and v_i are zero; V_0 is also expected to be zero. But if the output voltage even slightly deviates from zero, as is the case in practice, one percent of this deviation is transferred

to the non-inverting input, causing to increase in a fast rate the output voltage. The final state (either E^+ or $-E^-$) depends on the initial polarity of V_o.

The introduction of positive feedback thus results in the sharp transition between high and low output state represented in Fig. 2.1.4.A. For the circuit in Fig. 2.1.3, the gap width is 0.02V. When the output is in the high state, 10V for example, the input voltage sufficient to cause a high to low output transition must be more than -0.01V to pull the voltage at the noninverting input below zero. The similar consideration shows that the input voltage greater than 0.01V is required for the low to high transition.

Fig. 2.1.3:

Discriminator with positive feedback



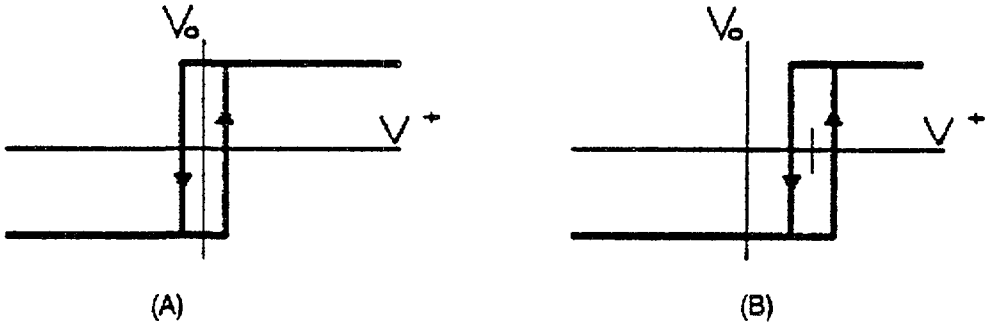
Increasing the input resistor R_1 and decreasing the feedback resistor R_2, increases the influence of the output voltage V_0 The hysteresis gap also becomes wider. Finally, the transition points can be shifted left and right by the proper choice of the V_{ref} voltage (Fig. 2.1.4.B).

Consider the modified discriminator pulse response. The discriminator level V_{ref} should be equal to the amplitude of the incoming pulse. The output pulse in the modified version is still of finite width while in the original version the output pulse width goes continuously to zero (Fig. 2.1.5).

An additional advantage of the hysteresis is the clear recognition of the zero crossing for slow varying signals in the presence of noise or hum (Fig. 2.1.6).

Fig. 2.1.4:

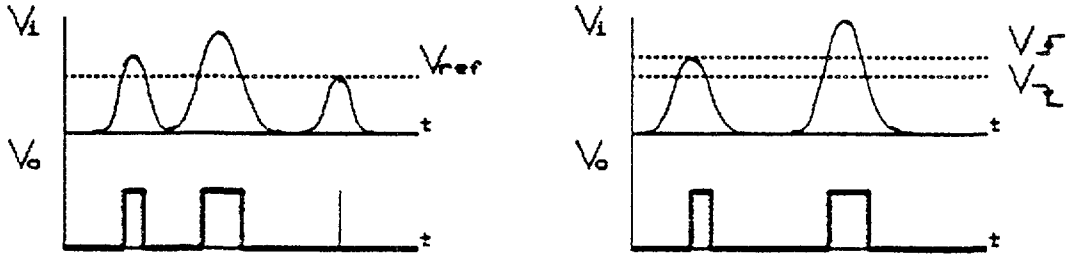
Input-output relation for circuit of Fig. 2.1.3 with (A)V_{ref} = 0 V (B)V_{ref} = 3V



In nuclear electronics, specially designed circuits for the pulse discriminator are used. They are faster than operational amplifiers due to faster recovery from saturation. Output voltage swings between 3.5 V and -0.5 V. Some typical representatives are 710 with a response time of 10 ns, LM 360 (14 ns), LM 311 (200 ns), TL 510 (30 ns) and Am 685 (6 ns, fastest but expensive).

Fig. 2.1.5 :

Effect of hysteresis on output pulse width.



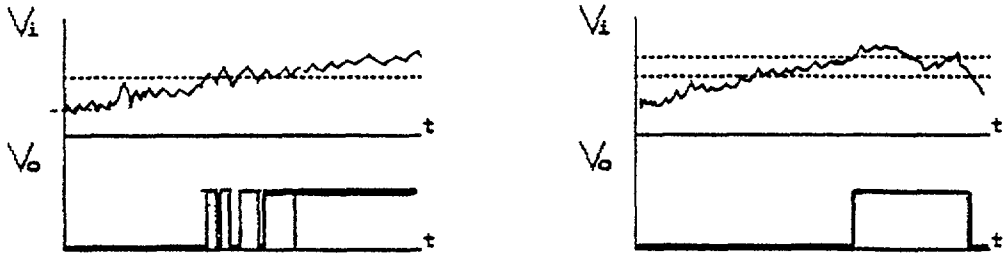


Fig. 2.1.6:

Using hysteresis to avoid multiple triggering.

EXPERIMENT

When assembling the printed circuit board according to Fig. 2.1.7 leave the 100K resistor out. Use the triangular input voltage and display simultaneously the input and output signals for different types of operational amplifiers: 741, LF 356, LF 357 and CA 3130 (for the last one the operating voltage should not exceed 12 V). . Prove that slowly varying signals give uncertain response when passing the V_{ref}.

Display the output voltage versus the input voltage in the X-Y oscilloscope mode. Verify the curves shown in Fig. 2.1.2, (A) and (B). Then insert the feedback resistor and verify the curves shown in Fig. 2.1.4, (A) and (B). Find the proper resistor and V_{ref} for hysteresis giving the up transition at 10 V, and down transition at 0 V.

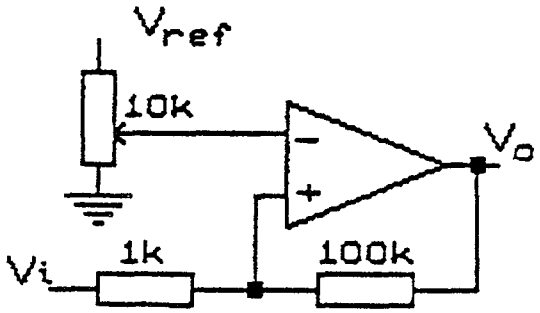


Fig. 2.1.7:

Circuit diagram of a discriminator.

The transition times are not identical for all different amplifiers. The fastest output rise time expressed in V/μs is called slew rate. Estimate slew rates for different amplifiers.

Typical slew rates range between 0.5 V/μs for the 741 (very slow), through about 10 V/μs for the LF 356 (typical value for modern operational amplifiers), to about 1500 V/μs for the NE 531 (very fast).

Notes:

EXPERIMENT 2.2

INVERTING AND NON-INVERTING AMPLIFIERS

OBJECTIVE

The basic properties of operational amplifiers are demonstrated. Special attention is given to a circuit based on a summing amplifier with weighted inputs used as a two bit digital to analog converter.

REVIEW

The operational amplifier (op amp) is one of the most remarkable and easy to use circuit elements developed. It is most used in the form of an integrated circuit containing the equivalent of hundreds of components. A simple circuit symbol shown in Fig. 2.2.1 represents this complex circuit The circuit is best treated as a black box into which one can put signals and out of which the desired signal can be taken.

The ideal amplifier has an infinite gain, infinite input impedance, zero output impedance, and infinite bandwidth. The remarkable thing is that practical circuits approch these ideal characteristics rather closely.

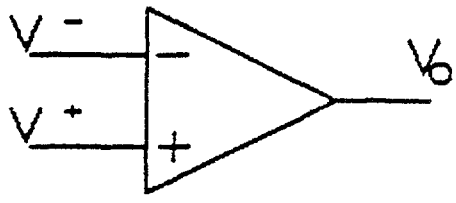


Fig. 2.2.1: Operational amplifier.

The circuit symbol leaves much to the imagination. The power leads are often not shown. Power is usually supplied by a bipolar symetrical power supply, often at +/- 15 V DC. All voltages and signals are measured with respect to a circuit ground which is never shown. Some frequency compensation lines are often omitted and not used in many circuits.

The open circuit gains of many types easily exceed 100,000. Input impedances of FET input op amps exceed 10^{13} ohms. Input currents vary from about 80 nA for a type 741 to 70 pA for the LM 356. Output impedances in typical circuits are of the order of a fraction of an ohm, although an unbuffered op amp might be capable of only 10 mA output current. Bandwidth can be quite narrow and is one of the pracitcal limitations of real op amps. High gain circuits might be limited to a few hundred Hertz. Low gain circuits can have bandwidths from DC to 100,000 Hz. Special but still inexpensive op amps will extend their usable upper frequency limit to 10^8 Hz.

This near approch to ideal permits first order design to proceed on the basis of two "golden rules".

1. The potential difference between the two input lines is zero (infinite gain).
2. The current into the op amp through the input leads is zero (infinite input impedance).

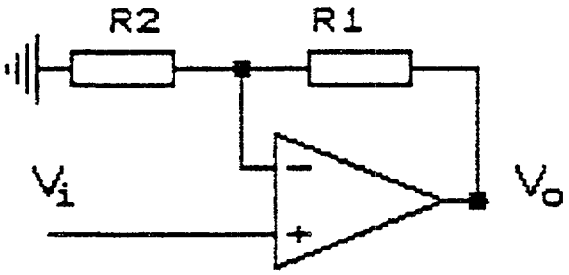


Fig. 2.2.2:

Non-inverting amplifier.

With these rules in mind, consider the first circuit in Fig. 2.2.2, the non-inverting amplifier.

The first rule means that the voltage on the inverting lead (marked with the - sign) is the same as the input voltage, Vi, on the non-inverting lead (marked with the + sign). The second rule says that there is no current into the non-inverting input so that

$$Vi = Vo\ R2 / (R1 + R2)$$

rearranging gives

$$Gain = Vo / Vi = 1 + R1 / R2$$

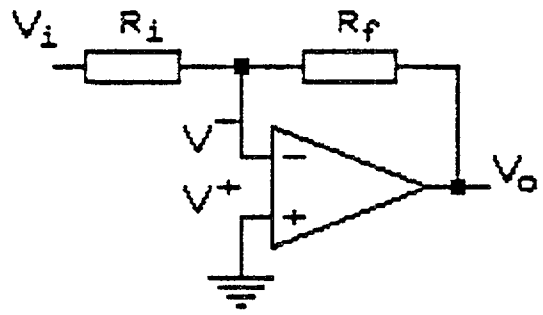


Fig. 2.2.3:

Inverting amplifier.

Another useful circuit is the inverting amplifier shown in Fig. 2.2.3.

In this circuit the first rule insures that the voltage at the inverting input is zero. Indeed that lead becomes a virtual ground. The second rule ensures that the current through Ri and Rf is the same. Thus

$$Gain = Vo / Vi = - Rf / Ri$$

The - sign indicates that the output is the inverse of the input, hence the name given to the circuit.

A useful circuit based on the non-inverting amplifier is the voltage follower shown in Fig. 2.2.4.

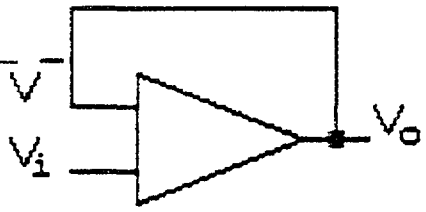


Fig. 2.2.4:

Voltage follower.

This circuit is just that of Fig. 2.2.2 with R1 = 0 and R2 = ∞ so that the gain is clearly 1. This circuit still has utility, however, because the high input impedance demands currents of only 80 nA (for a 741) to 70 pA (for a LM 356) while providing up to about 15 mA at a low output impedance.

The circuit in Fig. 2.2.5 is based on the imverting amplifier of Fig. 2.2.3. Here there are two inputs. Because the inverting input is at (virtual) ground, they are isolated from each other. Furthermore, the output of the circuit will be the sum of the inputs (weighted by the individual input gains). Use the golden rules to develop a formal equation for the output of this summing amplifier.

Note that the gain of one input is twice that of the other. This circumstance permits the circuit to be used as a two bit digital to analog converter with the most significant bit placed on the input with the highest gain.

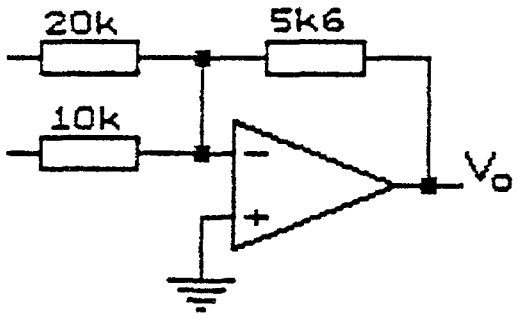


Fig. 2.2.5: Summing amplifier.

EXPERIMENT

Build the circuit shown. Note that in this case the gains are all less than one. This circumstance permits you to assign the binary value of 1 to the positive supply voltage and the binary value of 0 to ground. There are then four different possible input combinations, (0,0), (0,1), (1,0), and (1,1). Record the output voltage for each of these inputs. How could you make this circuit into a three bit D to A converter? (Note: you will have to change the overall gain of the circuit. Why?) Estimate the largest number of digital bits that a circuit of this type will accommodate.

Remove all inputs but one. Observe the pulse response of the operational amplifiers LF355, LF356, and 741 in this circuit. Set the pulse amplitude from 1 to 10 V with the repetition rate as high as possible and the pulse duration from 0.5 μs to 10 μs. Very sharp input pulses will be smoothed due to insufficient gain at high frequencies. The effect will be more pronounced if the gain is increased to 100 by replacing the feedback resistor of 5K6 with a 1M resistor. (The amplitude of the input will have to be reduced too.)

Notes:

EXPERIMENT 2.3

INTEGRATOR WITH RESET

OBJECTIVE

The operation of an active integrator is demonstrated by using dc and rectangular input signals. For the integrator reset a field-effect transistor (FET) is used and its typical properties are pointed out.

REVIEW

The circuit as shown in Fig.2. 2.1 performs the time integration of the input voltage V_i.

$$V_0 = -\int \frac{V_i}{RC}\,dt$$

If a small constant voltage of -100 mV is applied to the input of our circuit with R = 1 M and C = 10 nF, the ramp voltage V_0 will be produced.

$$V_0 = \frac{10^{-1}}{10^{6}\times 10^{-8}} \times t = 10\,t$$

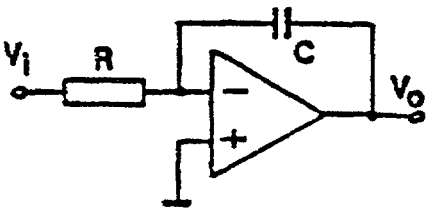


Fig. 2.3.1: Voltage integrator.

Starting from $V_0 = 0$, the saturation voltage of 10V will be reached in 1 second. To restore the initial state, the capacitor should be discharged. One way to do this is to introduce the n-channel FET 2N3819 as the analog switch (Fig. 2.3.2). When the FET gate is connected to the negative power supply voltage -V, drain-to-source channel is nonconductive ($R_{off} = 10^9$ Ohm). When the gate voltage is made close to zero by grounding the left side of the 10K resistor, the FET is made conductive (R_{on} = some ohms to some 100 R).

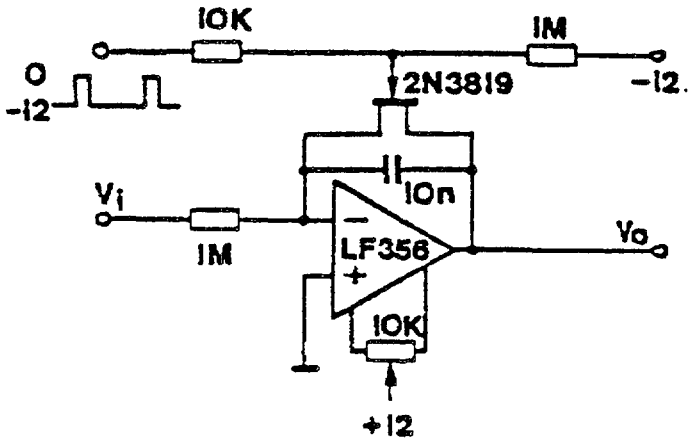
Saturation of the integrator amplifier may be avoided by connecting a large value resistor R_f across the feedback capacitor as shown in Fig. 2.3. In this case the integrator response to a dc input voltage vc is limited to $-(R_f/R)V_c$. Therefore, with the input grounded an output voltage close to zero is achieved. After this modification the integration of ac signals of frequency f is still correctly performed if the relation $2\pi f R_f C >> 1$ is fulfilled. In the opposite limiting case, when $2\pi f R_f C << 1$ the circuit is an amplifier with the gain of $-R_f/R_i$.

EXPERIMENT

After assembling the circuit drawn in Fig. 2.3.2, check the operation of the integrator with the grounded input. The expected output voltage V_0 should be zero. However, the observed voltage tends to slowly increase or decrease. Therefore, the exact zero of the integrator should be set by turning the potentiometer and observing the output voltage to get the stable output.

Fig. 2.3.2:

Integrator with reset.



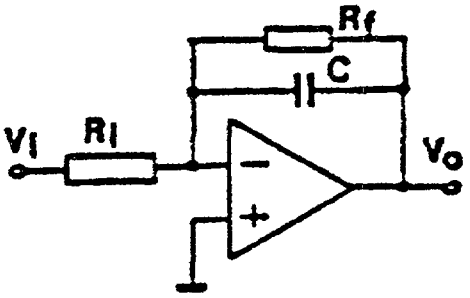
To prove the integration, a small input voltage of the positive or negative polarity should be applied. The saturation level of V_0 is easily reached. If the voltage is decreasing, the saturation level is observed at approximately -6V. This effect is caused by the FET which starts to conduct if its drain voltage exceeds one half of the gate voltage which is -12V.

If the rectangular voltage is applied to the input, the expected output voltage is of the triangular form. However, a ramp-stepped voltage signal is superimposed to the triangular output voltage until the integration is stopped either by the positive or the negative saturation level. This can be explained either by the DC component present in the input signal or by the input offset voltage instability.

Prove that the integrator becomes stable when 20 M (=10 + 10) resistor is connected across the feedback capacitor (Fig.2.3.3). Try to find the minimal frequency f of the rectangular input signal where the triangular output signal is still undistorted. How much is the term $2\pi f R_f C_f$ in this case?

Fig. 2.3.3:

Integrator with DC resistive feedback..



EXPERIMENT 2.4

SIGNAL AND PULSE GENERATOR

OBJECTIVE

The described signal and pulse generator provides rectangular and triangular voltage up to 10 V peak to peak in the frequency range from 2 to 2000 Hz. From the separate output periodic positive pulses of the variable amplitude 0 to 10 V, and the variable duration 1 to 14 μs of the same frequency as above are delivered.

REVIEW

The triangular and rectangular signal generator can be made by connecting the discriminator with hysteresis and an integrator in the closed loop (Fig. 2.4.1).

The operation of the circuit can be understood by assuming the low state of -10V at the discriminator output. Therefore the integrator output voltage linearly grows in time until the discriminator upper transition point is reached. Then the discriminator output voltage jumps into the high state at 10V approximately. Due to the integration of the positive input signal, the integrator output voltage descent linearly until the lower transition point is reached. After the discriminator output voltage is changed back to the low state, the cycle is over.

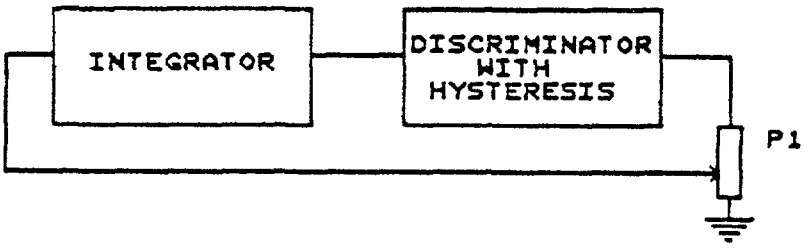


Fig. 2.4.1: Triangular and rectangular signal generator.

The frequency of the generated signals can be regulated by reducing the amplitude of the rectangular signal before the integration. Small input amplitude will result in a slowly increasing slope of the generated triangular voltage, and a long time will be needed to reach one or other transition point.

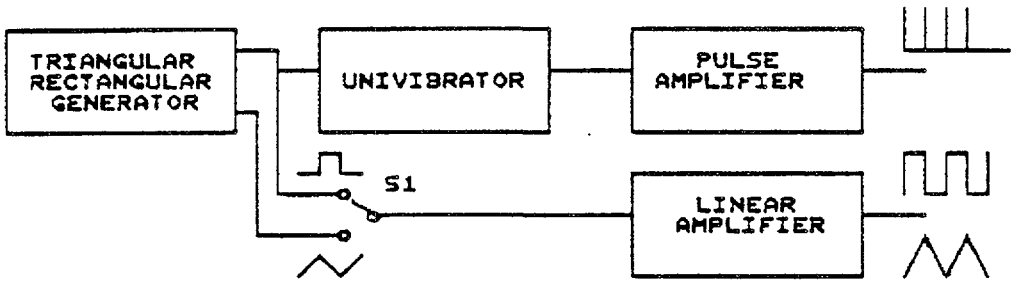
The triangular voltage is obtained at the output of the integrator, and the rectangular at the output of the discriminator. The desired voltage form is selected by the switch S_1 for the amplification in the linear output stage with the variable gain. In this stage the operational amplifier is used as a noninverting amplifier.

Having the triangular and rectangular voltage the circuit reading can be extended to the additional functional blocks (Fig. 2.4.2). The analog signals are amplified in the linear noninverting amplifier. For the pulse generation the positive edge triggered univibrator is used, and amplitude of the generated pulses is controlled by using the pulse output amplifier.

The already familiar building blocks can be recognized in Fig.2.4.3. The frequency of the triangular and rectangular signals can be varied in two ways. Continuous amplitude adjustment is achieved through potentiometer P_2 in the range 1:100.

Fig. 2.4.2:

Block diagram for the signal and pulse generator.



The operation of this system is poorly defined if the rectangular signal is attenuated more than 100 times. Below these values the amplitude of the attenuated rectangular signal becomes comparable with the input off-set voltage drift of the integrator. Therefore the lower part end of the dividing potentiometer is separated from the ground by a 100 R resistor. Coarse frequency adjustment is achieved by an additional capacitor which can be connected in parallel to the 10 nF capacitor in the integrator.

Because the triangular and rectangular signals are not equal in amplitude they are

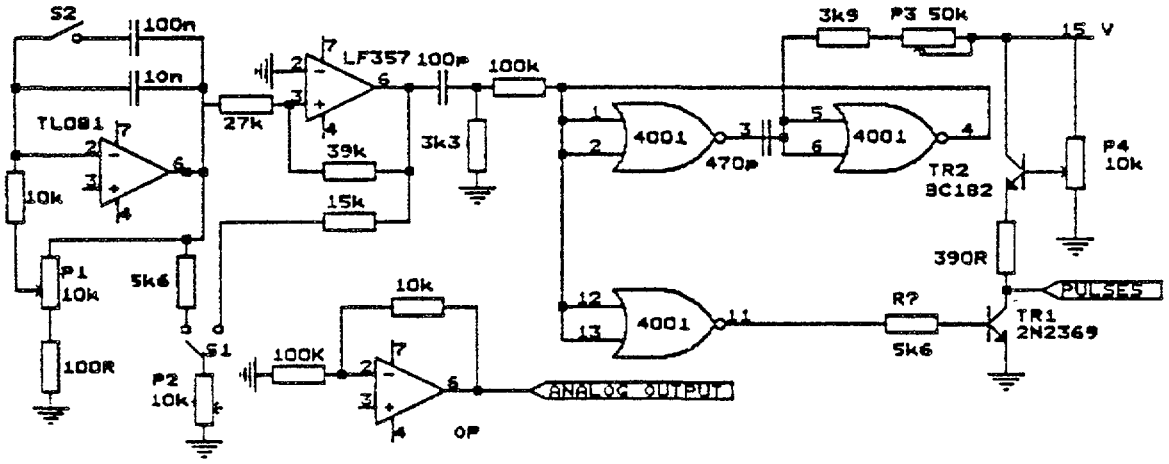


Fig. 2.4.3:

Signal and pulse generator

connected to the input of the noninverting amplifier through the equalising resistors 5k6 and 15 k. The output noninverting amplifier with a gain of 2 provides the output signals of amplitudes 10 V peak to peak.

The positive edge triggered univibrator activated by the rectangular input signal and serving for the pulse generation is explained in Experiment 3 "Univibrator". The variable resistor in place of R2 varies the output pulse duration. To get the positive pulses from the one-transistor amplifier the univibrator positive pulses are inverted before being applied to the base of the output transistor Tr1. This transistor is either fully conductive with a large current sink capability, or fully closed. In the latter case the output impedancy is 390 R, the value of the collector resistor. In this switched operation, the height of the output pulses is determined by the supply voltage i.e. the voltage at the emitter of the transistor Tr2. Due to the variable voltage on the base of this transistor, any value for the amplitude of the output pulses between 0 and the supply voltage can be set.

Before starting the assembling procedure, it is advisable to check the printed circuit board for the broken lines or for short circuits. Assembling starts with jumpers. During the assembling it is useful to check the operation of the separate stages.

EXPERIMENT

The discriminator and the integrator are first assembled, and their operation is checked. Then the noninverting amplifier is made and checked. Finally the univibrator is assembled and signals at pins 4 and 11, CD 4001 are verified.

If the generator will not operate, very probably the careful visual inspection of the soldered board will reveal one or few unsoldered points. It is also useful to check supply voltages at all corresponding IC pins (12 V at pin 7 for all operational amplifiers, and pin 14 for DC; -12 V at pin 4 for all operational amplifiers, and ground at pin 7 for CD).

Notes:

EXPERIMENT 2.5

SAMPLE AND HOLD

Properties of the sample and hold circuit are illustrated. Some parameters important for its operation are discussed and compared with the observations.

OBJECTIVE

A sample and hold circuit takes samples of the input voltage when the control pulse is applied and keeps it until the next control pulse arrives. The input - output relation of the circuit is illustrated in Fig. 2.5.1. Its operation is achieved by charging the capacitor C through the analog switch S as illustrated in Fig. 15.2.(a). The voltage across capacitor C follows the voltage V_0 when switch S is closed and remains constant when it is open. Of course, the output voltage V_i cannot be used without being changed due to the current taken out from the capacitor during the observation. By selecting a large C the performance of the sample and hold circuit could be improved. In this case, however, the output voltage V_o could not follow the input voltage during the fast sampling due to the finite switch resistance R_s through which the capacitor is charged.

REVIEW

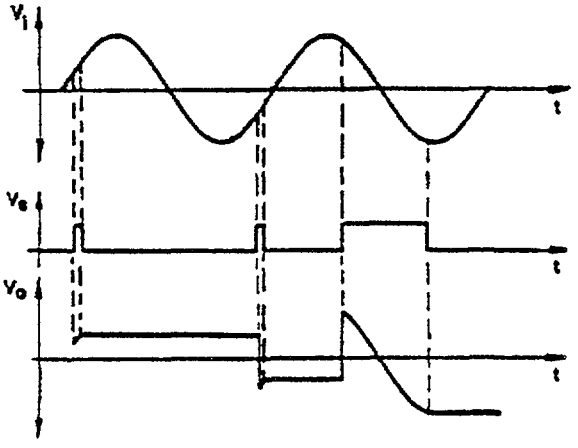
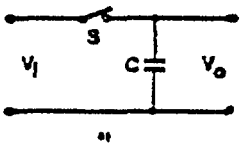


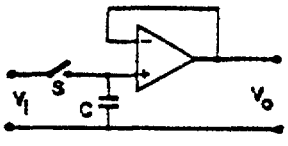
Fig. 2.5.1: Sample and hold wave forms.



a)

Fig. 2.5.2: Sample and hold basic diagram.

To avoid the use of the large capacitor, the voltage follower is added (Fig. 15.2b). When using LF 356 the current taken out from C does not exceed 10^{-10}A, and the output current capability is 25 mA.



b)

It will be interesting to estimate the characteristics of this circuit assuming the 5 V voltage across a 10 nF capacitor with the switch S open. In this case the voltage drop due to the amplifier bias current taken out from the capacitor will be 1 mV in 1 sec. If the analog switch contained in CD 4066 is used, the corresponding time constant determining the circuit time response will be $R_2C = 300.10^{-8}s = 3\,\mu s$. The sample pulse duration should not be

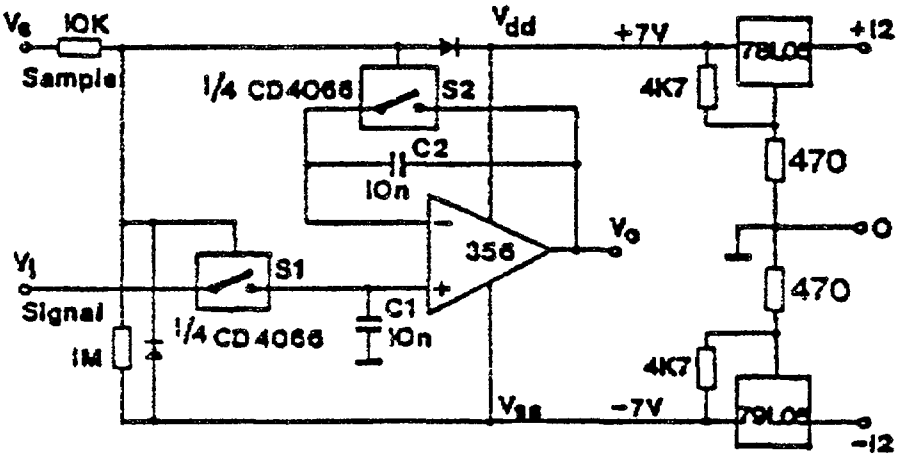
smaller than 5 RC. This will reduce the relative difference between the input and the output voltage at the beginning of the sample pulse to less than 10^{-2}. In our case this amounts to 15 μs. The practical circuit is drawn in Fig. 2.5.3.

The newly introduced components achieve two improvements. By using the second semiconductor switch, S2, the influence of the capacitive coupling of the sampling signal on the output signal is compensated. In addition, when switches S_1 and S_2 are open, the same current is taken from the identical capacitors C_1 and C_2, and therefore the effect of the bias current is compensated. Only the difference between bias currents, called the offset current is responsible for the output voltage drift. Thus the output voltage drift is, in general, 10 times smaller.

The operating voltage of the quad analog switch CD 4066 is limited to 15 V and therefore the +12/-12 V supply voltages are reduced to 7.5/-7.5 V by using three terminal regulators 78 L05 and 79 L05. The control input for the logical switches, also sensitive to voltages beyond the supply voltage range, is protected by two additional small signal diodes. When the CD 4066 control signal input is connected to a logical low state, the switches are open.

Fig. 2.5.3:

Sample and hold practical circuit.



Connect a sinusoidal signal o fa few volts amplitude and 1 kHz frequency to the input of the assembled circuit and observe the input and output voltage simultaneously. Then connect the sample input to the V_{dd} voltage to close the switches. The output will follow the input the voltage until the switches are opened. At that time the output voltage will remain at the value present when the switches were opened. Record the values of 50 sequential readings and plot their height distribution. Can you explain the result? What is the expected result if a rectangular voltage is sampled?

Apply periodic pulses of the frequency 1 kHz and duration of 10 μs to the sample input and adjust their amplitude to get an adequate logic signals at the gate of the CD 4066 switches.

Apply a sinusoidal or triangular voltage signal to the analog input and observe the output with a sampling frequency very close to the signal frequency. This technique permits fast signals to be converted into the sinusoidal signals. The observed effect is called the stroboscopic effect. Try to explain it.

Connect a constant voltage to the signal input and observe the output voltages. Decrease the frequency of the strobed pulses from 1 kHz to a few Hz and compare observations made with the LF 356 and the LM 318. Estimate the input offset currents for both amplifiers.

EXPERIMENT 2.6

DIFFERENTIATION AND POLE-ZERO CANCELLATION

OBJECTIVE

To demonstrate the approximate differentiation, used in first stage of the spectroscopy amplifier. If the spectroscopy amplifier processes pulses from the charge sensitive amplifier with the resistive feedback, the pole-zero cancellation circuit has to be added for the adequate pulse shaping.

REVIEW

The typical signals from an optically coupled charge sensitive amplifiers are shown in Fig 2.6.1. The information about the energy of the registered radiation is the height of the separate steps of the staircase voltage. A typical step height is a few tens of milivolts, and the staircase voltage range is from -5 V to +5 V. Such voltage can not be amplified without overloading the amplifier. Therefore the staircase voltage is differentiated. For the differentiation we can use passive RC circuit shown in Fig.2.6.2. Due to the nonexact differentiation performed by the RC differentiator, the resulting pulses are followed by the exponential curve approaching zero with the time constant RC. By the proper choice of the time constant, pulses with arbitrary width can be produced. The pulse width can be selected according the experimental conditions. The higher the counting rate the shorter pulses are desirable.

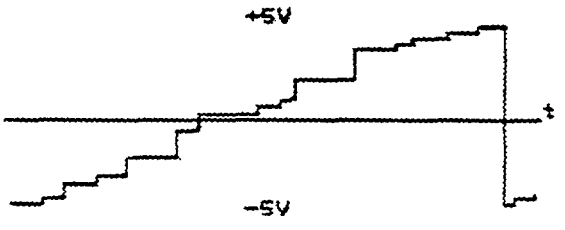


Fig. 2.6.1:

Output signal from an optical feedback preamplifier.

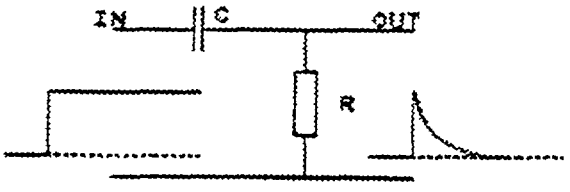


Fig. 2.6.2:

Passive differentiation.

Another type of the charge sensitive preamplifiers uses the resistive feedback. Their output signal is shown in Fig.2.6.3. The typical decay constant is from 15 to 50 us, at the same amplitudes than above. Such pulses would not overload spectroscopy amplifier. Nevertheless, we have a good reason to differentiate them, as well. Because of the long exponential tail following each pulse, two or more pulses can be superimposed. This leads to the erroneous pulse height registration. This effect is called the pileup effect. To make pulses shorter and reduce the pileup effect we can differentiate pulses from the preamplifier but the result is given in Fig.2.6.4. Pulses are followed by the undershoot. This undershoot approaches zero exponentially, with the

Fig. 2.6.3:

Output signals from resistive feedback preamplifier.

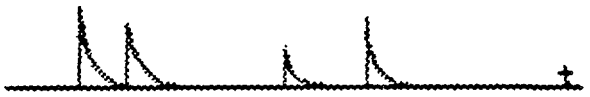
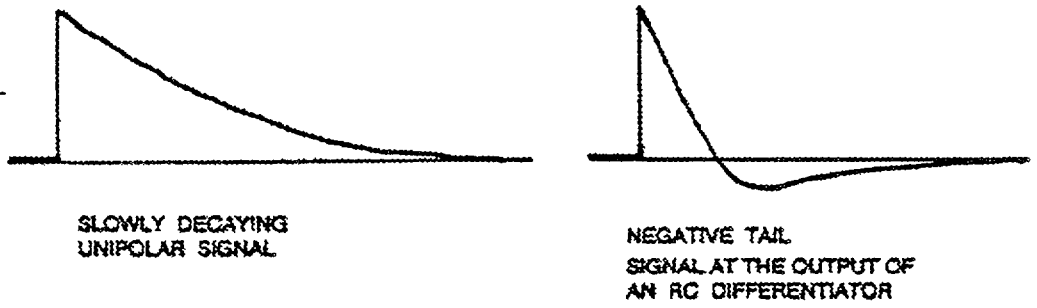


Fig. 2.6.4:

Effect of pasive differentiation



time constant RC which is equal to the time constant of the input pulses.

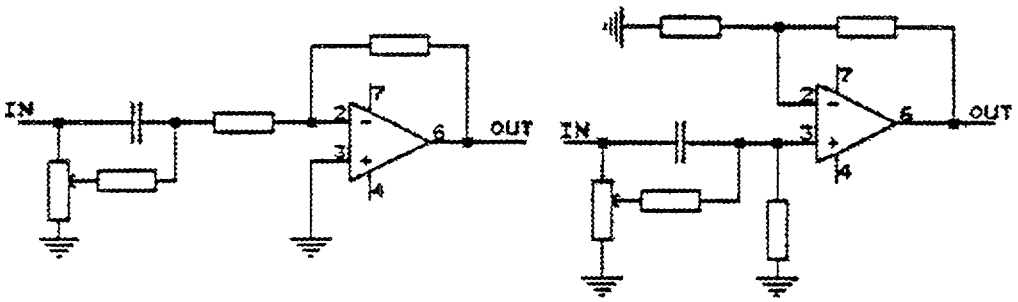
The pileup effect will appear again, although less pronounced. However, the undershoot can be removed by using the pole-zero compensating circuit.

First, the idea of the pole-zero compensation will be explained, by using the intuitive approach.

The undershoot to be eliminated is exponential, with the time constant τ of the input pulses but much smaller than the corresponding exponential tail in the input pulse. If we add the adequate part of the input pulse to the differentiated pulse, both exponential tails of the opposite polarities cancel each other.

Fig. 2.6.5:

Two circuits for polezero cancellation.



Circuit shown in Fig.2.6.5.provides the required combination.

To prove this procedure with some mathematics, we will follow Figs. 5.6.6, 5.6.7 and 5.6.8.

We know the transfer function D(s) of the approximate differentiator making exponential function from the step function (Fig.2.6.6). Therefore, if we want to return the exponential function back into the step function, the unit with the inverse transfer function 1/D(s) should be used (see Fig.2.6.7). After passing both shaping, F(s) and G(s), the output function should follow the input function. Therefore the transfer function of both serially connected units should be unity. The second one, G(s), is the inverse of the first one, F(s).

In Fig. 2.6.8, the exponential function with the time constant τ is applied to the input of

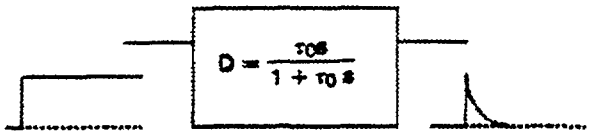


Fig. 2.6.6.:

Passive differentiation.

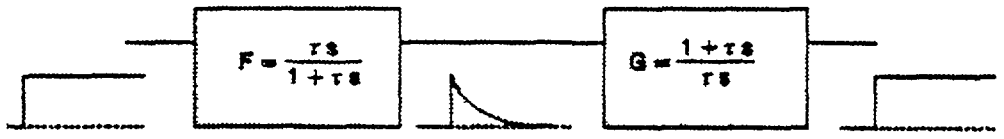


Fig. 2.6.7:

Pasive differentiation followed by its inversion.

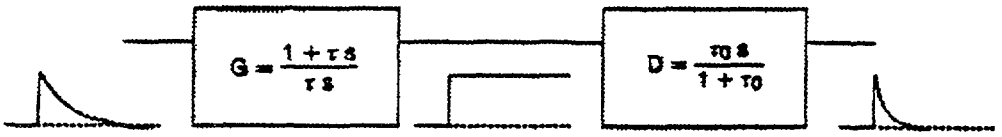


Fig 2.6.8:

Shaping of one exponential to another.

the unit with the transfer function G(s). There it is shaped into step function. By adding the approximate differentiator with the transfer function D(s), the exponential pulses of the new width τ_0 are generated at output. The input unit of the spectroscopy amplifier should have the transfer function

$$G(s)\,D(s) = \frac{1 + \tau s}{1 + \tau_0 s}.$$

To verify differentiation and the pole zero cancellation, the circuit shown in Fig. 2.6.9. will be used.

EXPERIMENT

Assemble the circuit and apply the rectangular voltage of a few kHz and 1V peak to peak to the input. Observe the output pulses of U1. The following stage (the amplifier and the polarity inverter) realised with U3, does not change the pulse shapes. For the proper operation, the tap of the potentiometer should be in the ground position. Observe the effect of the applied input voltage to the output signal when you lift the tap.

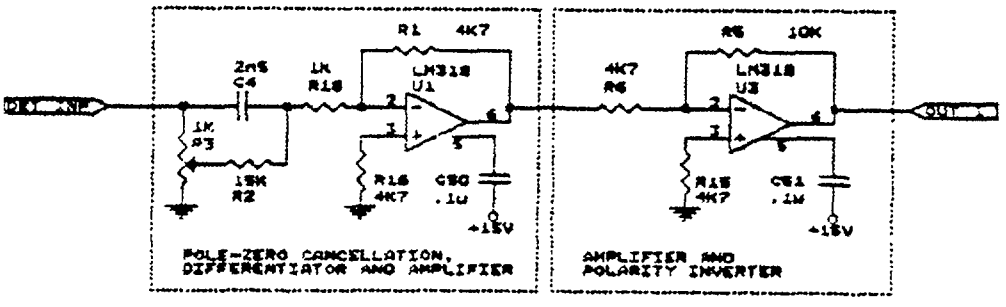


Fig. 2.6.9:

Differentiation and polezero cancellation circuit.

Prepare the circuit which will simulate the signals from the charge sensitive amplifier with the resistive feedback (Fig. 2.6.10.). TTL pulses of duration of 400 ns are applied to the input charge capacitor C1 through the diode D1. The exponential voltage across C1, because of its discharge through the resistor R3, approaches zero with the time constant of about 50 μs. The exponential voltage is repeated through the voltage follower using U2.

Apply the produced pulses to the differentiator and observe effect of the pole-zero cancellation.

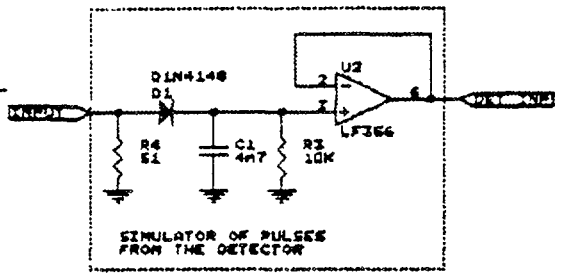


Fig. 2.6.10:

Exponential pulse generator.

Experiment 2.7

COMPLEX POLE FILTERING

OBJECTIVE

In an advanced spectroscopy amplifier, the pulse shaping is a delicate process. The basic concepts of a complex pole shaping are presented. The comparison between "classical" RC shaping and the complex pole one is made.

REVIEW

After amplification the pulses in a nuclear spectroscopy amplfier have shapes as shown in Fig. 2.7.1. To improve the signal to noise ratio, S/N. these pulses are filtered in filter F. The signal to noise as close as possible to the optimal value ratio will be if pulses at the filter output have Gaussian shape. In the early days of nuclear physics, filters with a transfer function

$$Ts = \frac{1}{(1 + \tau s)^n}$$

(n from 2 to 4) are used. However, the resulting pulse shape were far from Gaussian (Fig. 2.7.2). Later filters with transfer functions with complex poles was introduced. A second order filter with two complex poles is the well-known resonant circuit. The response of such a filter to any pulse is a damped oscillation. The main pulse is followed by a set of pulses with decreasing amplitudes. It seems that such filters could not find application in nuclear spectroscopy. However, the serial combination of two such filters, tuned to frequencies fo and 2fo, and almost critically damped, provides nearly Gaussian output pulses.

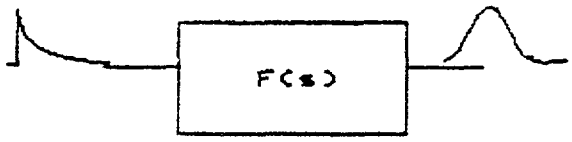


Fig. 2.7.1: Desirable pulse shaping.

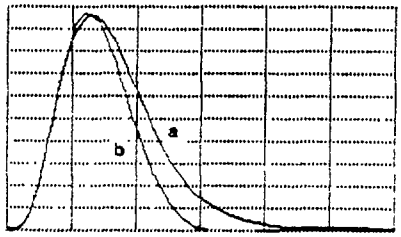


Fig. 2.7.2: Semigaussian pulse shaping: a) Four approx. integrations b) Complex poles, fourth order.

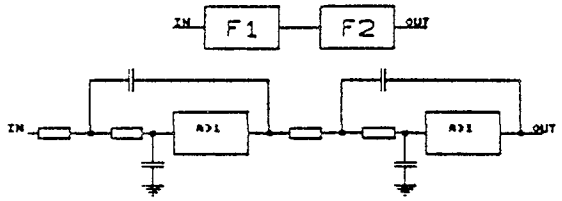
In practice we do not use tuned circuits. The required function is achieved by two active filter of the second order (Fig 2.7.3). The filter performance depends on the amplification A of the amplifier used. If A = 1 then we have a classical filter with critical damping. With A up to 3 the output oscillations will increase. At A = 3 circuit will start to oscillate.

EXPERIMENT

Assemble circuit shown in Fig. 2.7.4 and study its operation by using different amplifier gain settings (P1 and P2). Try to find the optimal pulse shaping. The output pulse should be as symmetrical as possible, and followed by an undershoot which can be observed only by using larger vertical amplification on the oscilloscope sensitivity.

Fig. 2.7.3:

Fourth order filter: block diagram.



Pulses with the exponential tail should be used as the input signal. Such pulses are produced from the rectangular voltage, by circuit given in Fig. 2.7.5. The time constant should match complex pole filter characteristics (Fig. 2.7.6). Pay attention to the exact selection of resistor and capacitor values.

Fig. 2.7.4:

Wiring diagram.

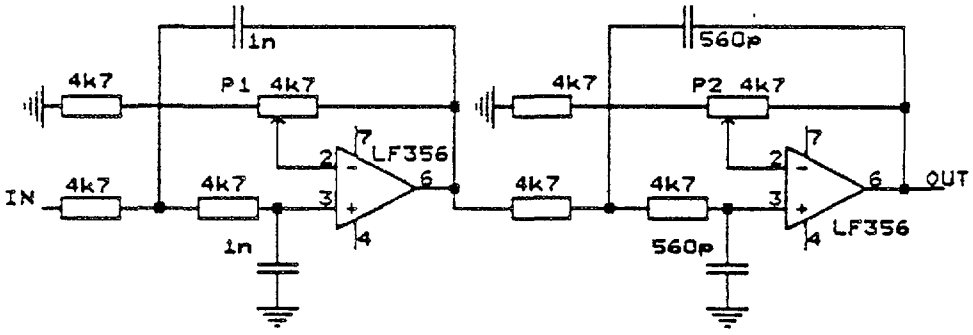


Fig. 2.7.5:

Proper position of complex poles.

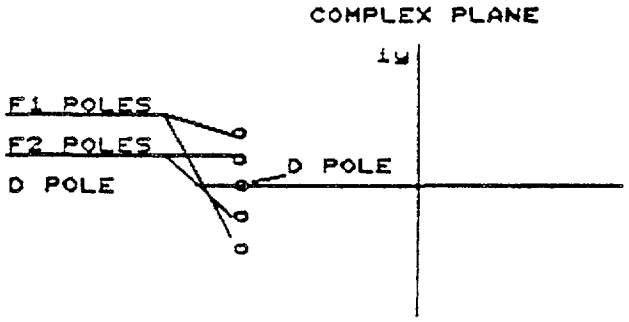
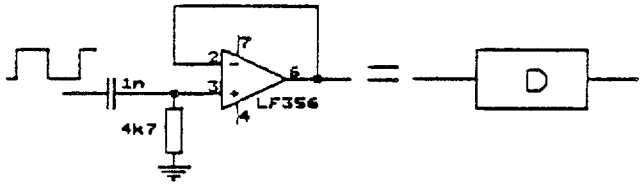


Fig. 2.7.6:

Exponential pulse generator.



EXPERIMENT 2.8

BASELINE RESTORER

OBJECTIVE

Baseline restorer concepts is discussed. The properties of the gated and the ungated versions are compared, and verified by an experiment.

REVIEW

The circuit shown in Fig. 2.8.1 has the tendency to keep the output voltage z at zero regardless of the constant voltage x applied to the input. Let's try to understand why this is so.

If the nonzero voltage x is applied to the input the output will be Ax. This voltage is integrated by the integrator with the sign inversion. The resulting voltage is applied to the input of the amplifier and superimposed on the voltage x. Because the polarity of the integrated output signal is inverted, the new resulting output voltage z will be smaller. The integrator output voltage will still rise but in a slower manner, and the resulting output voltage will go to zero slower and slower. Finally, the output voltage z will be zero, at any constant input voltage x. The descend to the zero will follow an exponential curve.

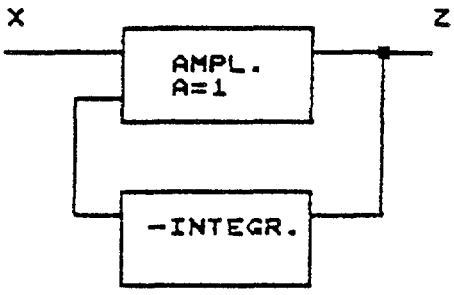


Fig. 2.8.1: Simple baseline restorer (BLR).

A clearer insight into operation of the above system is obtained if some mathematics is applied.

At the output of the integrator the voltage will be $-(1/\tau s)\,z$, as the response to the input voltage. This voltage together with the input voltage x will give at the amplifier input: $x - (1/\tau s)\,z$. This voltage, amplified A times, will be equal to the output voltage z.

$$A\left(x - \frac{1}{\tau s}\right) z = z$$

For the output voltage we get:

$$z = A\,\frac{\tau s}{1 + \tau s}\,x$$

For low frequencies, the term in denominator τs is small compared with 1, and can be neglected. In this case the input-output relation is:

$$z = \tau s\, x$$

The input signal is differentiated. Therefore the output voltage z will be zero if the input voltage x will vary slowly. On the other hand, for fast input signals, 1 is small compared with τs. The resulting output is:

$$z = A x$$

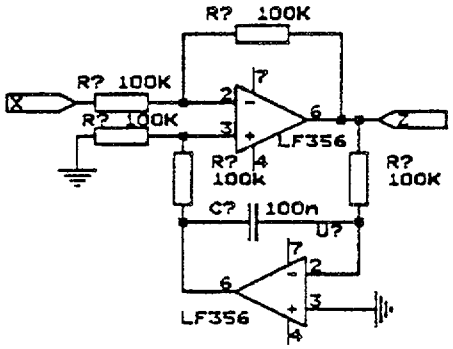
The conclusion is that the DC component is removed while the superimposed pulses will remain unaffected. This is the aim of the base line restorer.

EXPERIMENT

If we build the system according to Fig. 2.8.2 we will observe the output signal with the deviated base line even when the input signal should not need correction (Fig. 2.8.3). Our base line restorer does not work as expected. Its behavior can be explained by discussing its transfer function.

Fig. 2.8.2:

Realization of BLR.

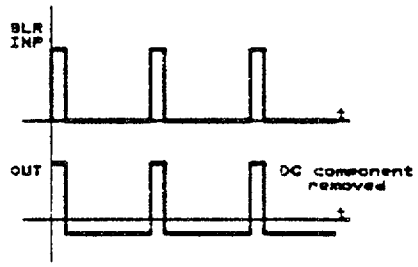


$$T = A s/(1 + s)$$

This transfer function is identical with the transfer function of the approximate differentiator shown in Fig. 2.8.4. If the time constant is big, the signal will go through unaffected, with the DC component removed. This means that even a pulse train with the exact zero voltage between pulses, applied to the the input circuit, will be pushed down, as observed.

Fig. 2.8.3:

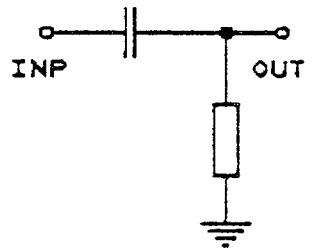
Effect of differentiation on the baseline.



The desired BLR operation is achieved if the base line is observed during intervals without pulses. The output z is disconnected from the integrator input by adding the FET 2N3819 as an analog switch (Fig. 2.8.5). Gating pulses of -12 V are applied to the FET gate during the pulse appearance. One way to produce proper signal and gating pulses is shown in Fig 2.8.6. The collector voltage of the pnp transistor swings from -15V to +3.5 V (710 output). The proper swing of the gating voltage is adjusted by potentiometer P1. Even in this case the base line is not of the right value. Investigation with the pulse input grounded, and gating pulses applied, reveals the output voltage z shifted in the positive direction by an amount proportional to the rate of the gating pulses.

Fig. 2.8.4:

Pasive differentiator



This effect can be explained by the reverse current into the gate, and the corresponding integration. The effect can be cured by introducing a second FET compensating the described effect. The second FET is connected to the integrator noninverting input as shown in Fig. 2.8.7.

It may still happen that the BLR will not operate satisfactory if the same pulses will be applied to the input X and the gating input. The gating intervals partially overlap because of the delay in the gating line. Special measures are undertaken in spectroscopy amplifier to solve this problem.

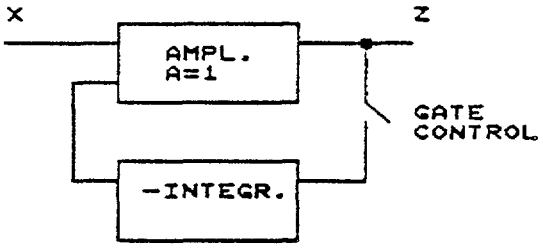


Fig. 2. 8.5:

Proper gating

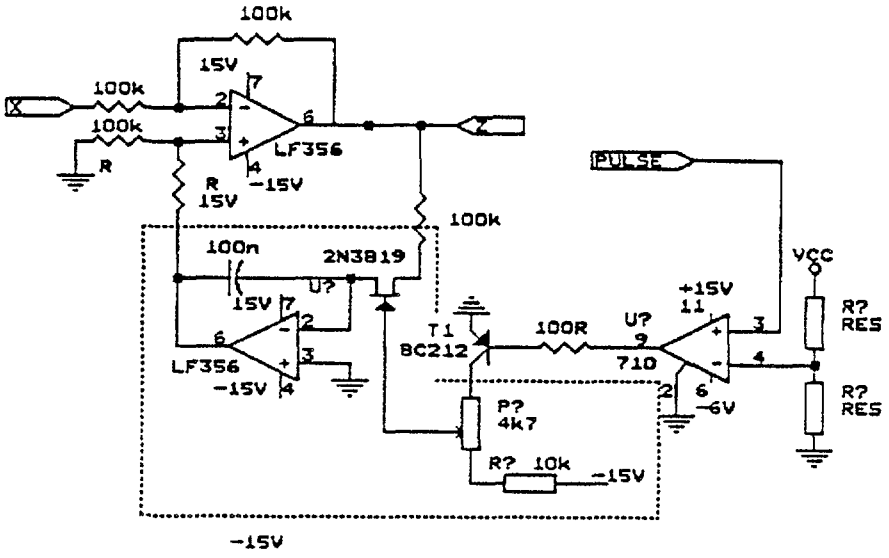


Fig. 2. 8.6:

Improved BLR circuit

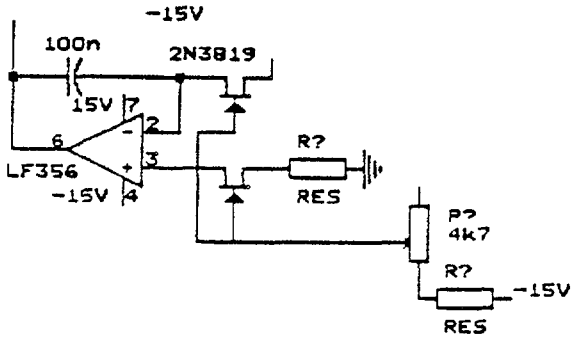


Fig . 2.8.7:

Compensation of the FET gate current.

Notes:

Experiment 2.9

SIMPLE SPECTROSCOPY AMPLIFIER

OBJECTIVE

The experiment provides for investigation of the basic properties of a spectroscopy amplifier with professional design properties. By adding more features such as a selectable time constant and additional gain ranges, it can be used in the laboratory.

THEORY

A good spectroscopy amplifier performs two functions. First, it increases the amplitude of the signal delivered by the preamplifier, to the level required by the further processing instruments, such as multichannel analyzers. Secondly, it maximizes the signal-to-noise ratio, by enhancing frequencies in the signal spectrum, and depresing noise frequencies. The amplifer must provide for a stable, count rate independent baseline, as tne signal amplitude is to be measured between peak and baseline. The amplifier must be able to produce unipolar output pulses, while receiving input pulse with an exponential decay.

The amplifier, the circuit of which is shown in Fig.2.9.1, has three gain and pulse shaping stages, built around IC1, 2 and 3, an active baseline restoration network built around IC4 and an output buffer, IC5. Pole-zero cancellation is effected at the amplifier input.

Gain and Pulse Shaping Stages

The incoming signal is expected to have an exponential decaywith a time constant of around $\tau = 50\,\mu s$. To avoid pile-up and other problems this signal is to be shortened.

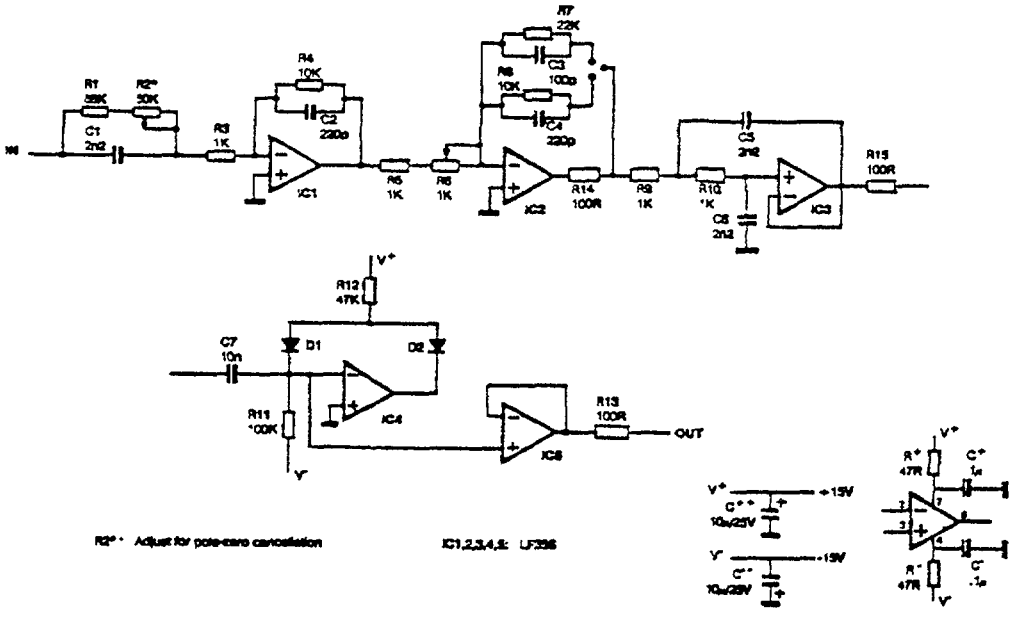


Fig. 2.9.1: Wiring diagram.

This is done by active differentiation with a time constant essentially determined by C1 and R3, $\tau_{diff} = 2.2\,\mu s$. However, to eliminate signal undershoot, a pole-zero cancellation technique is used; potentiometer R2 is to be adjusted to make C1 · (R1 + R2) = τ, the decay time constant of the input signal. Decay constants from 150 μs to 260 μs can thus be cancelled. (The differentiation time constant is, more exactly, given by C1 · R3 / (R1 + R2); this differs from C1 x R3 by less than 2% even if R2 = 0).

An active integration is also performed around IC1 by the feedback network C2 - R4, with a time constant $\tau_{int} = 2.2\,\mu s$. When the pole-zero network is adjusted, the gain of the first stage is seen to be 10/e (e = 2,78).

The second stage uses the same feedback configuration as the first one. It performs a $\tau_{int} = 2.2\,\mu s$ integration and provides for variable gain setting both continuously, by a factor varying between 1 and 2 through adjustment of potentiometer R6, and in a step, by a factor of 2, by choosing the feedback network. The maximum DC gain of this stage is given by -R7/R5 = −22. The AC gain is smaller due to the integration time constant.

The third amplifying stage has unity dc gain and performs a double integration with a time constant $\tau_{int} = 2.2\,\mu s$. The output buffer, which receives the signal from the baseline restorer described below is followed by R13, a 100R resistor used for impedance matching to a coaxial cable with Z_o = 93R. The output current is limited by IC5 to about 15mA.

Altogether the amplifier performs one differentiation and four integration. All the time constants are equal to 2.2 μs. Thus the amplifier gives a quasi-gaussian shape to an incoming exponentially decaying signal. This is a very appropriate shape to obtain a good signal to noise ratio in a spectroscopy system.

Baseline Restorer

The active baseline restorer works to keep a zero voltage at the inverting input of IC3 (a fast operational amplifier); this node is connected to the input of the last amplifying stage. The restoration is made necessary because a capacitor (C7) has been used to cancel the large DC gain of the amplification chain (amplifier plus preamplifier). Signals of either polarity whose amplitude exceeds a very small value cut off one of the diodes D1 (positive signals) or D2 (negative signals). When this happens C7 is charged with a current of roughly -120 μA. This has a very small effect on the amplitude of the signals, which are of short duration. By unbalancing the currents in D1 and D2 while there are no pulses present, the restorer is able to keep the value of the voltage at the buffer input very close to zero even for reasonably high count rates.

As shown in the schematics, all the integrated circuits are connected to the power line trough RC decoupling networks. This is important to avoid oscillations and interactiopns between the various circuits. The networks should be physically close to the IC, and the capacitor soldered to a good ground line. The LF 356 is an FET input operational amplifier with a gain bandwidth of 5 MHz and a slew rate of 12V/μs; it has a low noise input voltage and a typical offset voltage of 1 mV.

EXPERIMENT Assemble the spectroscopy amplifier, observing the components layout as shown in Fig. 2.9.2. Then start with testing as follows:

1. Check for spurious oscillations by looking at the output with a scope.

2. Observe the behaviour of the amplifier by confirming with a DVM that the voltages at the inputs and outputs of the different operational amplifiers have the expected values. The input to the whole amplifier should be shorted to ground. Then, approximately 0 V will be measured at those nodes.

3. Connect the charge sensitive preamplifier to the input and use a pulse generator to inject a charge pulse into the preamplifier. The output of the preamplifier should be a signal of about +0,5V amplitude with very short rise time and decaying exponentially with a time constant of around 220 μs.

4. Reduce the signal to a level that will give a 5V output signal at maximum gain. Check that the amplifier is not saturated. Observe the signal shape at the output of IC1 (one differentiation plus one integration), the output of IC2 (two integrations), and the output of IC3 (four integrations). Measure the gain of these stages; check the gain controls.

5. Observe the signals at the input and output of IC4. It is seen that, while the (positive) input signal is on, IC4 saturates to the negative rail making D2 conduct all the current that passes through R12 while R11 slowly charges C7.

6. Observe the amplifier behaviour when it is overloaded and compare its behaviour to the one observed when the pole-zero cancellation network is not adjusted.

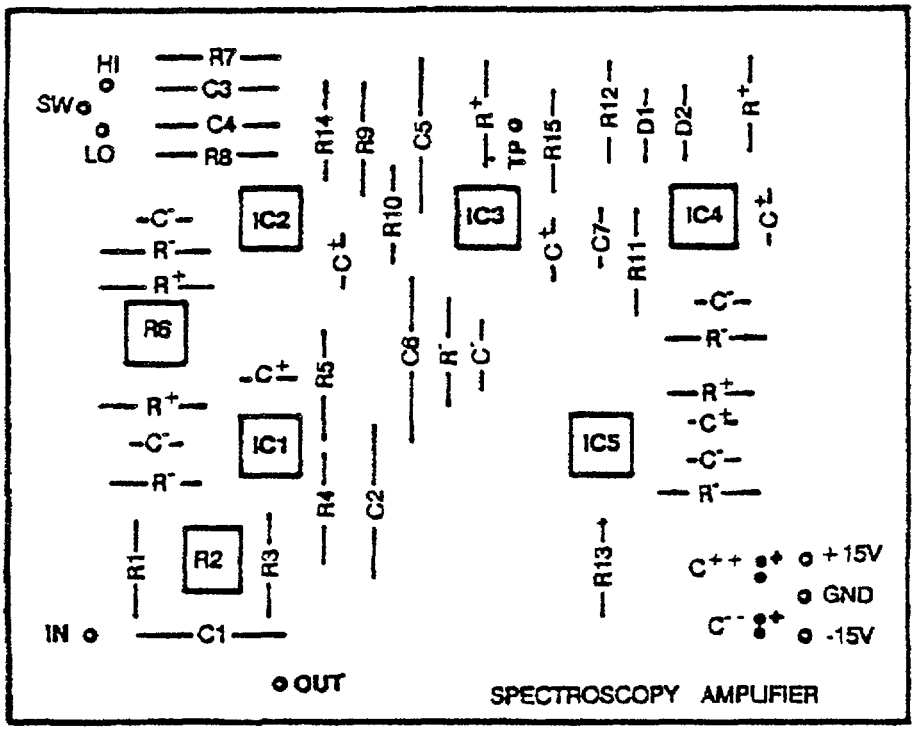


Fig. 2.9.2:

Components layout for Experiment 2.9.

Notes:

Experiment 2.10

SELECTING A FET

OBJECTIVES

The resolution of a high resolution nuclear spectroscopy system strongly depends on the noise generated within the electronic data processing linear system. The contribution of the FET used at the input of the charge sensitive amplifier is dominant. The exercise describes how to measure FET parameters that define its noise figure. Its knowledge enables the selection of the most suitable FET out of a batch.

REVIEW

In a normally operating charge-sensitive preamplifier, the dominant noise contribution is the thermal noise in the channel of the input field-effect transistor and to reduce this term as much as possible, a field-effect transistor with a large transconductance g_m should be selected.

The transconductance increases as the drain current in the field-effect transistor is increased. However, it has to be borne in mind that the drain current cannot exceed a value, called I_{DSS}, which represents the value of the current flowing into the drain when gate and source are at the same potential.

The selection of a FET for minimum noise operation proceeds as follows. Making use of the circuit of Fig. 2.10.1, measure the I_{DSS} values for all the transistors you have received. I_{DSS} should be determined by making sure that the drain-to-source voltage lies within +5 and +6V. In this way, each component will be characterized by its I_{DSS} value. The next step will be the measurement of the transconductance g_m. The circuit of Fig. 2.10.2 will be used for this purpose.

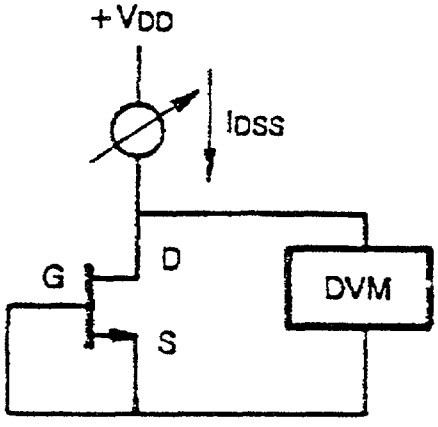


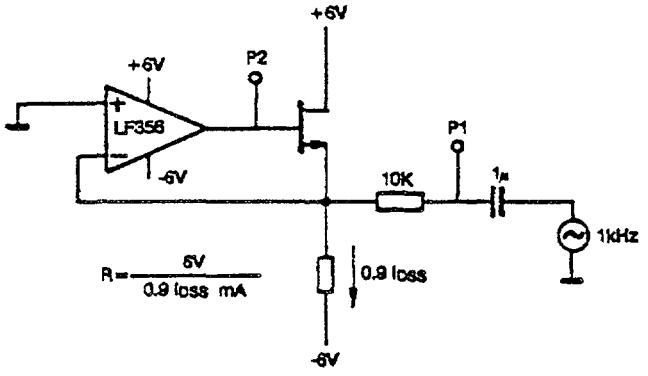
Fig. 2.10.1: Measuring I_{DSS}.

In this circuit, the feedback loop keeps the source of the FET at 0 V. In this loop the source of the FET behaves as a very low impedance input. The steady current in the FET is set to a value of 0.9 IDSS by choosing the resistor R connected between the source of the JFET and the -6V supply according to the relationship:

$$R = \frac{6V}{0.9\, I_{DSS}} \quad [kOhms]$$

Fig. 2.10.2:

A circuit to measure the transconductance.



where I_{DSS} is expressed in mA. Obviously, different values of R will be required for FETs of different I_{DSS}.

EXPERIMENT

Connect then a 1 kHz sinusoidal oscillator through a 1μF decoupling capacitor and a 10k resistor to the source of the field effect transistor. Adjust the current flowing through the 10k resistor according to the following criterion. The peak-to-peak sinusoidal current entering the FET source must not exceed 10% of the DC value. Therefore, the amplitude control of the sinusoidal oscillator must be set so as to meet the previous requirement. In other words, the peak-to-peak voltage at P1 read with an oscilloscope, divided by 10k must give a current equal to 10% of 0.9 IDSS, that is equal to 0.09IDSS. Let us call this peak-to-peak current i_s. Flowing into the source of the FET, i_s modulates the gate-to-source voltage. Read the peak-to-peak value of the sinusoidal voltage at the output of the operational amplifier. Let us call this peak-to-peak voltage v_G. The ratio i_s/v_G gives the value of the transconductance.

An example will clarify the whole procedure. Assume an FET for which the measurement of Fig. 2.10.1 gives an I_{DSS} of 8 mA. The transconductance will therefore be measured at 90% of I_{DSS}, that is, at a standing current of 7.2 mA. A source current of 7.2 mA must therefore be used in the circuit of Fig. 2.10.2. The value of the unknown resistor R is

$$R = \frac{6V}{7.2\ mA} \approx 820\ [Ohms]$$

Having introduced this resistor into the circuit, you know that the DC source current in the field-effect transistor is 7.2 mA. Therefore, the peak-to-peak value of the 1 kHz sinusoidal current employed for the gm measurement must not exceed the value

$$0.1 \times 7.2\ mA = 0.72\ mA.$$

To fix this current, look at the sinusoidal voltage at P1 and adjust the sinusoidal generator amplitude until the voltage at P1 is 7.2V. Now you are sure that the current through the 10k resistor and entering the source of the FET is 0.72 mA. Now measure the peak-to-peak amplitude of the sinusoidal voltage at P2. Suppose, for instance, that this peak-to-peak amplitude is 120 mV. The transconductance is given by:

$$\frac{720\ \mu A}{120\ mV} = 5\ mA/V$$

The measurement of g_m has to be repeated on all the units available. Now each unit will be characterized by its value of I_{DSS} and its value of g_m. The FET with the largest g_m will be introduced in the charge-sensitive preamplifier.

EXPERIMENT 2.11

PREAMPLIFIER

OBJECTIVES

The purpose of the experiment is to assemble, and put to work a low noise, charge sensitive preamplifier, housed in a metal box. The preamplifier is of professional design, and can be used in nuclear experiment.

REVIEW

In a solid state detector, just as in the case of an ionization chamber, radiation looses its energy by producing charge carriers. The sum of these charge carriers, the total charge, is the primary information from the detector. This charge introduced into the detector capacity would give rise to a voltage signal. The detector capacity, however, is not constant. It is proportional to the square root of the supply voltage of the detector.

Therefore preamplifiers are used which are sensitive to the charge at the input. They convert the input charge to an output voltage. Thus the changes in the detector capacity no longer influence the amplitude of the output pulse. The appropriate circuit consists of a low noise, inverting operational amplifier with a feedback impedance, parallel connection of a resistor and a capacitor as shown in Fig. 2.11.1.

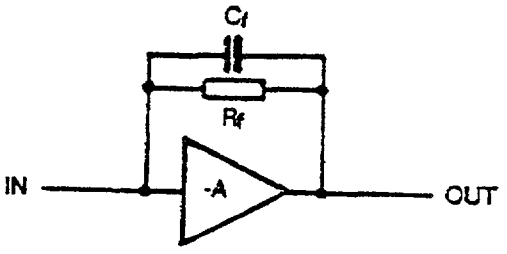


Fig. 2.11.1: Operational amplifier with feedback.

We now refer to the complete circuit diagram in Fig. 2.11.2. The preamplifier has two blocks. The first one (T1 - T4) is the charge sensitive loop, corresponding to the appoximate current integrator, shown in Fig. 2.11.1. The second amplifier(T5 - T9) provides voltage gain and a low output impedance.

Approximate quiescent values for voltages and currents at several points are shown in the diagram.The field effect transistor T1 provides low noise and high input impedance to the basic amplifier of the charge sensitive loop. The signal current developed in T1 flows through T2 and the high impedance offered by current source T3 acting as a load; this determines a high voltage gain in this stage. Resistors R4 and R6 and capacitor C3 avoid high frequency parasitic oscillations. The value of R3 will depend on I_{DSS}. Note that the current entering the current source T3 also passes through R3; thus R3 may be determined through the relation R3 = 7.6V/(2mA +0.9 I_{DSS}).Potentiometer R13 allows the output quiescent voltage to be adjusted to 0V through the application of a quiescent negative voltage of appropriate value to the gate of T1.The feedback impedance corresponding to C_f and R_f of Fig. 2.11.1, is the parallel combination of C2 and R2. Thus the input current is integrated in C2 and the corresponding voltage pulse has a decay time constant $\tau = C2 \cdot R2 = 220\,\mu s$.The second block is a voltage amplifying stage with the gain defined by the feedback resistor ratio, (R18 + R19)/ R18 = 5.7. Transistors T5, T6 and T7 constitute a cascode differential amplifier, R22 being the load resistor. T8 and T9 assure a large output current capability.

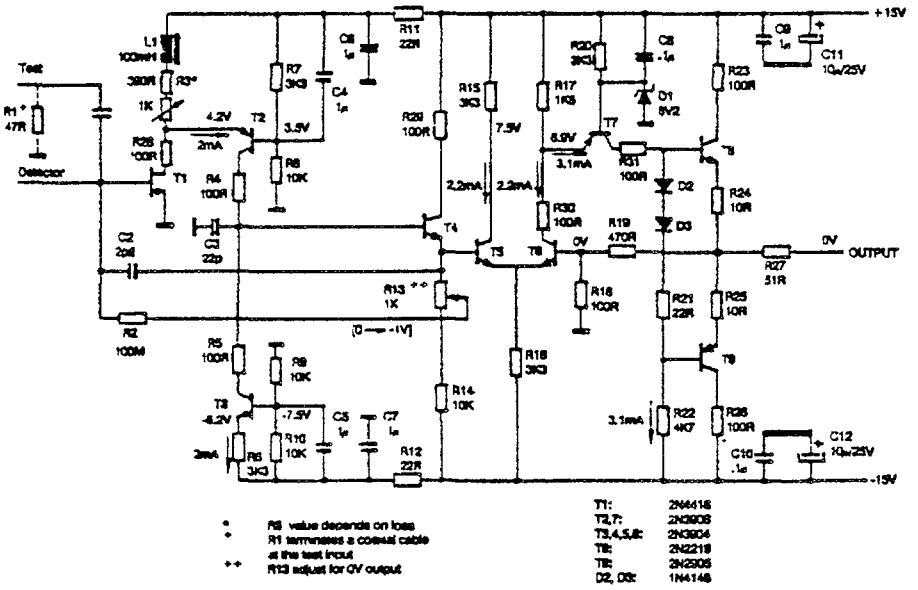


Fig. 2.11.2:

A circuit to measure the transconductance.

Feedback makes the impedance at the common node of R24 and R25 practically zero, and R27 is used to match the coaxial cable impedance.

EXPERIMENT

Once the layout of the charge-sensitive preamplifier shown in Fig. 2.11.3 is ready, check the DC voltages at all the circuit nodes. Compare the values of voltages you have found with those written in the circuit diagram.

If you are sure that the circuit works correctly from the point of view of the DC condition,

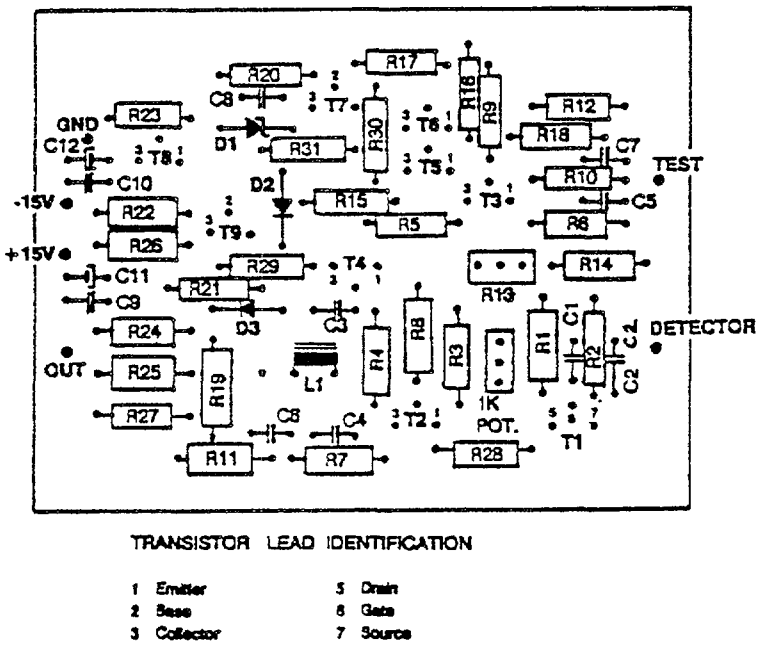


Fig. 2.11.3:

Components layout for preamplifier.

introduce it into the special metal box with which you have been provided with. Such a box acts as a shield, reducing the 50Hz pick-up which otherwise would make measurements very difficult.You are now ready to begin the analysis of the signal behaviour of your circuit. To do this, connect the generator to the test input and fix the following operating conditions for the test signal:

shape:	rectangular
polarity:	negative
amplitude:	100 mV
repetition rate:	100 pps
pulse width:	1 ms

Look at the output of the whole preamplifier and observe the shape of the signal. This should look like the one shown in Fig. 2.11.4.

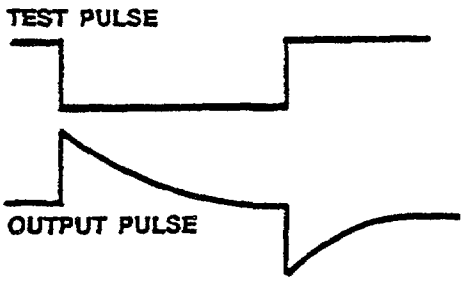


Fig. 2.11.4: Preamplifier output.

Measure the decay time constant of the exponential signal at the preamplifier output and compare the measured value with the product C2.R2 of the capacitance and the resistance in the feedback bipole of the charge-sensitive loop. If agreement exists between the nominal and the real values, within the obvious inaccuracy margin due to finite components tolerances, you can go to the next step. Measure the risetime as a function of a capacitance, which simulates the detector, connected across the input terminals of the charge-sensitive preamplifier.

A set of capacitors ranging from 20 pF to 300 pF is available for this measurement.

The measurement has to be performed as illustrated in Fig. 2.11.5. The detector simulating capacitor C_D is connected in the way shown in the figure. Raise the generator pulse rate to about 10^3 pps and measure the risetime of the output pulse for $C_D = 0$ at first and then for C_D = 20 pF, 50 pF, 100 pF, 150 pF, 200 pF, 250 pF, 300 pF. (Remember: risetime is defined as the time it takes the pulse to go from 10 % to 90 % of its maximum value.)Plot the measured risetime as a function of C_D.Connect then the 300 pF capacitor at the preamplifier input and double C_2, that is, increase it from 2.2 to 4.7 pF. Measure the risetime and compare the value just found with the one found before for C_f = 2.2pF and C_D = 150 pF.

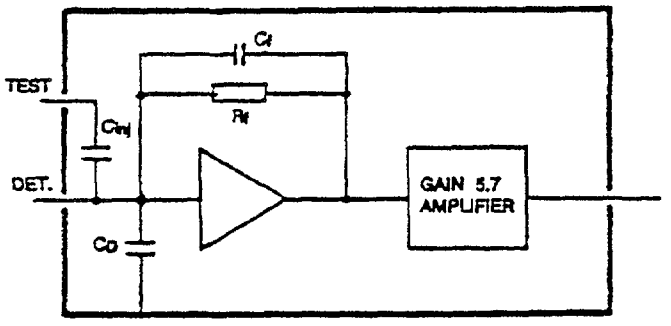


Fig. 2.11.5: Decay and risetime measurements.

Notes:

EXPERIMENT 2.12

NOISE MEASUREMENTS

OBJECTIVE

The energy resolution in high resolution spectroscopy is limited by the quality of the detector as well as by the noise from the electronic system. Both contributions are approximately balanced. Electronic noise is mainly generated in the input FET in the preamplifier, and is reduced by filtering in the last stages of the spectroscopy amplifier. In this experiment, simple methods for electronic noise measurement are discussed and verified.

REVIEW

With the preamplifier (see Experiment 2.11) and the simple spectroscopy amplifier (see Experiment 2.9) connected together and the whole system checked as far as signal behaviour is concerned, observations about noise can be made.

A short explanation about the ways of expressing noise at the input of a linear amplifier system for radiation detector signals will be given.

Remember that the radiation detectors employed in the energy measurements deliver a CHARGE which is proportional to the energy released by the ionizing radiation in the sensitive region of the detector. The noise introduced by the amplifier system can accordingly be expressed as

- NOISE CHARGE REFERRED TO THE PREAMPLIFIER INPUT, or as
- WIDTH, EXPRESSED IN UNITS OF ENERGY AND REFERRED TO THE DETECTOR OF A HYPOTHETICAL SPECTRAL LINE WHICH IS BROADENED BY THE PREAMPLIFIER.

It has to be born in mind that both ways express in different units the NOISE CONTRIBUTION of the preamplifier and for this reason the definition I is independent of the material employed in the detector (silicon, germanium, CdTe, HgI_2 and even gas). The preamplifier noise contribution, expressed according to second definition above, would depend on the material of which the detector is made.

The preamplifier noise is strongly dependent on the value of the capacitance C_D connected at the preamplifier input to simulate the detector as well as on the shaping implemented by the spectroscopy amplifier. Therefore, before starting the noise measurements, make sure that the set of capacitors you will use to simulate C_D have been accurately measured.

EXPERIMENT

Now, the way in which the detector current pulse is simulated has to be explained. Remember that a detector can be thought of as a current source, delivering a known amount of charge, in parallel with a capacitor. The capacitor is C_D. The current pulse will be simulated in the way shown in the Fig. 2.12.1. As already pointed out, a small injection

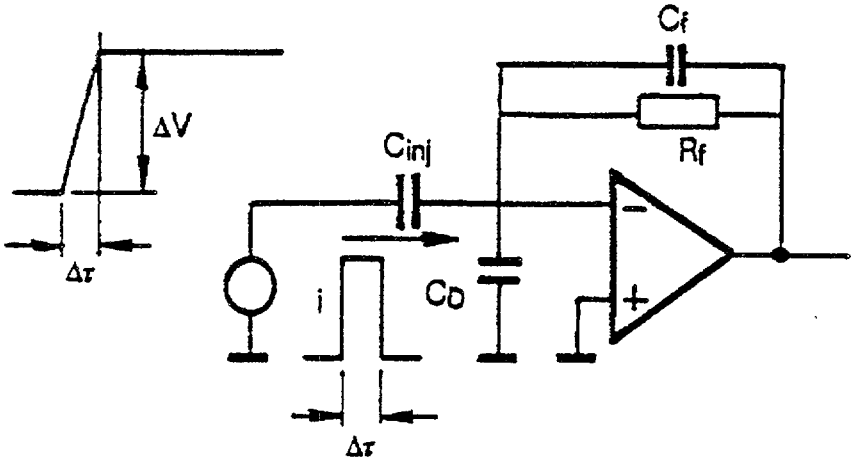


Fig. 2.12.1:

Simulating a current pulse.

capacitor, C_{inj}, is provided inside your preamplifier box. One terminal of C_{inj} goes to the preamplifier input, while the other one is soldered to a connector on the box wall, labelled TEST INPUT.

By applying to the test input a quasi-step signal with a finite slope on its leading edge, the current flowing through C_{inj} will be a rectangular pulse of width Δt, carrying a charge

$$C_{inj} \frac{\Delta V}{\Delta \tau} = \frac{\Delta Q}{\Delta \tau}$$

If C_{inj} is known in value and adequately stable, the charge injected ΔQ can be accurately controlled by the signal amplitude V.

This method enables the designer to simulate the radiation detector in a very accurate way. If the generator employed has provision for changing slope on the leading edge, the measurement can also account for the finite collection time in the detector, which is simulated by $\Delta \tau$. The latter possibility will not be studies here, for it is useful only for a second-order correction in the noise measurements and therefore will be neglected.

Become, then, familiar with the detector simulating charge injection and set the generator to the following conditions:

- REPETITION RATE: 1 kHz
- PULSE WIDTH: 100 μS
- PULSE POLARITY: *negative*

Set the minimum value of the gain in the spectroscopy amplifier. Estimate the charge injected by a 2.2pF injection capacitor when the voltage applied to it is 20 mV.

Pay due attention to the measurement of the input step amplitude and measure the amplitude of the signal which appears at the output of the spectroscopy amplifier. The measurement should be performed in the following way.

Use a T-junction connector at the test input of the charge-sensitive preamplifier. Connect through a coaxial cable the output of the pulse generator to one of the inputs of the T connector. Go with a coaxial cable from the other leg of the T connector to the channel-A

input of an oscilloscope and terminate there the coaxial cable on its proper characteristic impedance. As the impedance presented by the preamplifier test input is very large and purely capacitive, in this way you make a feed-through connection from the generator through the preamplifier to the scope. Use then a probe connected to the channel B of the scope to display the spectroscopy amplifier IC3 output. The whole method is illustrated in Fig. 2.12.2.

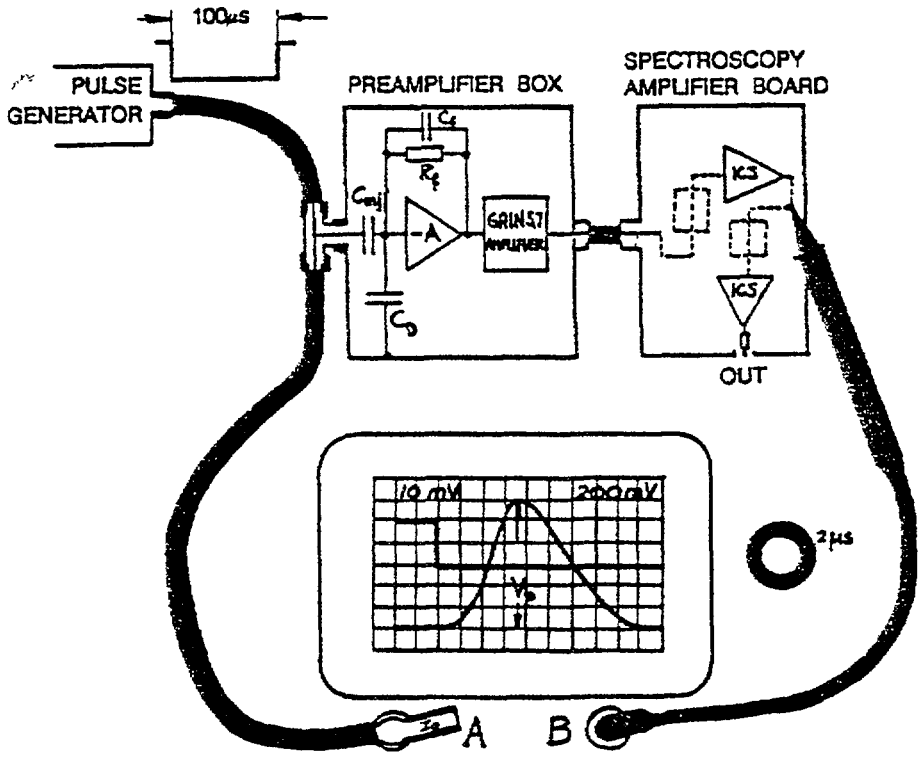


Fig. 2.12.2: Determine the charge sensitivity of the amplifier system.

Employ, as typical sensitivities for this measurement:

Channel A	vertical	5 mV/div	horizontal	2 - 5 μs/div
Channel B	vertical	200 mV/div		

Adjust the generator amplitude setting to make the amplitude of the step of channel A equal to 20 mV. This is a convenient value for the foregoing measurements. Note that 20 mV across a 2.2 pF injection capacitance generates a charge equal to:

$$2 \cdot 10^{-2} \cdot 2.2\,10^{-12} = 4.4 \cdot 10^{-14} \quad \text{C (Coulomb)}$$

$$\frac{4.4 \cdot 10^{-14}}{1.6 \cdot 10^{-19}} = 2.75 \cdot 10^{5} \quad \text{electrons}$$

As a unit of charge injected, remember that a 1 mV signal through a 1 pF capacitor gives

$$10^{-3} \cdot 10^{-12} = 10^{-15} \quad \text{C or}$$

$$\frac{10^{-15}}{1.6 \cdot 10^{-19}} = 6250 \quad \text{electrons}$$

Return now to the display you have on the scope, with the injected step on channel A and the semi-Gaussian signal taken at the output of IC3 on channel B. Using transparent paper pressed against the display of your oscilloscope, sketch the shape of the semi-Gaussian signal and mark on it the correct time scale. This will be used as auxiliary information to determine whether your preamplifier gives comparatively satisfactory results.

Determine now the charge-sensitivity of your spectrometry system. To do this, measure the peak amplitude V_p of the pulse delivered by the spectroscopy amplifier.

The charge-sensitivity of your system will then be the ratio between V_p and the amount of charge injected at the input. In the present case, the charge-sensitivity S_c will be expressed as:

$$S_c = \frac{V_p}{4.4 \cdot 10^{-14}} = 23 \ V_p/pC$$

$$S_c = \frac{V_p}{2.75 \cdot 10^{5}} = 3.6 \cdot 10^{-6} \ V_p/electron$$

For instance, if upon injecting 20 mV at the input (do not forget that the previous relationship assumes an input signal of 20 mV) you find V_p = 1V, then the charge-sensitivity of your system will be

S_c = 23V/pC or

$S_c = 3.6 \cdot 10^{-6}$ V/electron = 3.6 μV/electron.

The energy sensitivity of the system depends on the type of detectorwith which the system is intended to work. So, in association with a silicon detector where creation of an electron-hole pair requires 3.67 eV, the energy sensitivity of the system would be:

$$S_E = S_c \text{ / (energy to form a pair)} = \frac{3.6 \ \mu V}{3.67 \ eV} = 1 \ \mu V/eV \quad \text{or} \quad 1 mV/keV$$

of energy released.

If the detector connected to the system is, instead, germanium where 2.97 eV are required to create one electron-hole pair, the energy sensitivity of the system would be:

$$S_E = \frac{3.6 \ \mu V}{2.97 \ eV} = 1.2 \ \mu V/eV \quad \text{or} \quad 1.2 \ mV/keV$$

The noise measurement can now be performed. Two methods will be described here.

a) Measuring the RMS noise of the amplifier system and refering it to the input of the whole system.

This method has the advantage of rapidly leading to a preliminary estimate of the noise performances of the spectroscopy system. It can also be suitably accurate if a true RMS voltmeter, like the Hewlett Packard 3400 A is available (10 Hz - 10 MHz bandwidth). If

such a voltmeter is not available, a first approximation of the RMS value can be made in the following way.

Display the noise at the output of the spectroscopy amplifier on the oscilloscope with sufficiently high sensitivity so as to have the noise band covering at least two vertical divisions.

Observe the noise by changing the horizontal scanning speed. Make sure that no 50Hz pick-up is present and that no periodic spikes appear to be superimposed to the noise band, which must look homogeneous. Make sure that the dominant noise contribution, as it ought to be, is the one coming from the preamplifier. For this purpose, disconnect the preamplifier and terminate the input of the spectroscopy amplifier with a 93 R resistor. The noise appearing now at the output of the spectroscopy amplifier should be considerably smaller than the one observed previously with the preamplifier connected. If it is so, connect the preamplifier again and start the quantitative noise measurements.

Reduce the horizontal sensitivity to 10 μs/div and increase the beam intensity so as to be able to detect the peak-to-peak amplitude of the noise. Remember that the noise has a gaussian amplitude distribution where the following relationship holds:

$$\text{RSM value} \approx \frac{\text{peak to peak amplitude}}{6.6}$$

In this way you will find a value which represents in mV, the RMS noise at the output of IC3. The RMS value is related to the full width at half maximum (FWHM) according to the expression FWHM = 2.355 RMS value.

To determine the EQUIVALENT NOISE CHARGE referred to the input, that is, the noise charge which may be considered responsible for the measured output RMS noise, you have just to divide by the charge sensitivity of your system:

$$\text{EQUIV. NOISE CHARGE} = \frac{\text{output RMS noise}}{S_c}$$

The equivalent noise charge is usually expressed in ROOT MEAN SQUARE ELECTRONS. If, instead, you prefer to express the noise in terms of noise linewidth referred to input, this parameter being frequently referred to as energy resolution, observe that:

FWHM Output noise line = 2.355 RMS output noise.

Then divide FWHM output noise line by the energy sensitivity of your system. The result (FWHM output noise line) S_E, usually expressed in keV, gives the resolution of the system.

b) Measurement employing a multichannel pulse height analyzer

This method requires the pulse generator to be permanently connected and consists in displaying on a multichannel analyzer two Gaussian lines corresponding to two accurately known amplitude settings of the generator (see Fig. 2.12.3). The preamplifier noise smears the amplitude distribution of the pulses. This is the reason why two gaussian distributions are observed at the output of the amplifier system. The measurement procedure is as follows: adjust the generator amplitude setting until on channel A of the

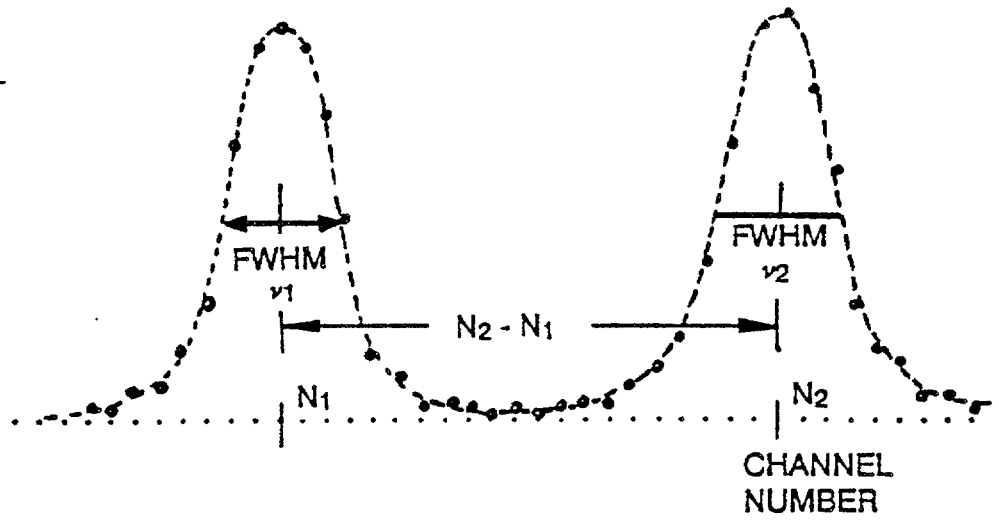


Fig. 2.12.3:

Energy resolution deplayed on a MCA.

scope you read the first reference amplitude which may be, as previously, 20 mV. Take now the real output of the spectroscopy amplifier, that is, the output of the IC5 buffer with the cable characteristic impedance in series, and connect it with a cable to the input of a multichannel analyzer. Accumulate the resulting gaussian noise distribution until the curve is well defined, that is, has small statistic fluctuations. It is advisable to choose the operating conditions in such a way that the noise line has a FWHM of at least 10 channels. Then stop the accumulation and introduce the second amplitude, which might be 40 mV. Check the amplitude of the generator accurately on channel A of the scope without changing the vertical sensitivity. Start accumulating the new gaussian line until it has approximately the same peak contents as the previous one. Then stop the multichannel analyzer and process the display information, shown in Fig. 2.12.3 in the following way.

Define by visual inspection the centroid positions of the two Gaussian lines and determine the order numbers N_1 and N_2 of the corresponding channels. As you know that the difference in the centroid positions was caused by a difference of 20 mV (40 mV - 20 mV) in the signal amplitude, and you also know that 20 mV across 2.2 pF simulates an equivalent energy in silicon of 1,000 keV, you can calibrate the energy axis of your multichannel analyzer, by observing that an input energy variation of 1,000 keV gives rise to a shift in the spectral line of $N_2 - N_1$ channels. The energy calibration is therefore

$$\frac{1000}{N_2 - N_1} \quad [\text{ keV/channel }].$$

Determine now the FWHM of the first and second Gaussian curves, and let ν_1 and ν_2 be their widths in number of channels.

The resolution for the first and second Gaussian lines therefore is

$$\frac{1000}{N_2 - N_1}\nu_1 \quad \text{keV, FWHM in silicon}$$

$$\frac{1000}{N_2 - N_1}\nu_2 \quad \text{keV, FEWM in silicon}$$

The FWHM in Ge is obtained by remembering that 20 mV across 2.2 pF in germanium simulates an equivalent energy of 810 keV and therefore the calibration coefficient would be:

$$\frac{810}{N_2 - N_1} \quad \text{keV/channel}$$

PAY ATTENTION: the FWHM should be the same for both spectral lines within the statistical fluctuations. If the values of ν_1 and ν_2 2 differ by more than 5%, there is a nonlinearity in the circuit.

Remember that in the noise measurement based upon RMS reading, the output from the spectroscopy amplifier has to be taken from IC3, to avoid baseline restorer induced distortions in the noise line. The measurement with the multichannel analyzer, instead, is made on the peak of the waveform resulting from the combination of signal and noise. The signal, accordingly, has to be taken at the true output of the spectroscopy amplifier.

Plan the noise measurements carefully so that you do not use too much multichannel analyzer time and thus delay the work of other groups. Measure the ENC using the oscilloscope at the values of C_D you have already employed for the risetime measurement, that is:

C_D = 0, 20 pF, 50 pF, 100 pF, 150 pF, 200 pF, 250 pF, 300 pF.

Check that the ENC value at $C_D = 0$ is less than 1,000 electrons RMS and that the slope is less than 20 electrons /pF. If your system is below the two upper limitations, you can go to the multichannel analyzer.

Determine finally the values of the resolution $(FWHM)_1$ for C_D = 100 pF and $(FWHM)_2$ C_D = 200 pF and the slope

$$\frac{(FWHM)_2 - (FWHM)_1}{100} \quad \text{keV/pF}.$$

Notes:

EXPERIMENT 2.13

DIGITAL SETTING OF AMPLIFIER GAIN

OBJECTIVE

To demonstrate the method which permits the gain of a feedback amplifier to be digitally set by an analog switch. An FET is used as a switch, and the experiment shows how to control the FET when the voltage at its terminal can change widely.

REVIEW

Several applications in the field of data acquisition require amplifiers for which the gain can be preset for example by a computer instruction, or more generally, by applying a digital word to the gain control input.

In the present circuit, which is a non-inverting operational amplifier in the non inverting connection, the gain is changed by switching a resistor in the feedback loop.

A single bit word in this case selects the desired value of the gain. The principle is shown in Fig. 2.13.1.

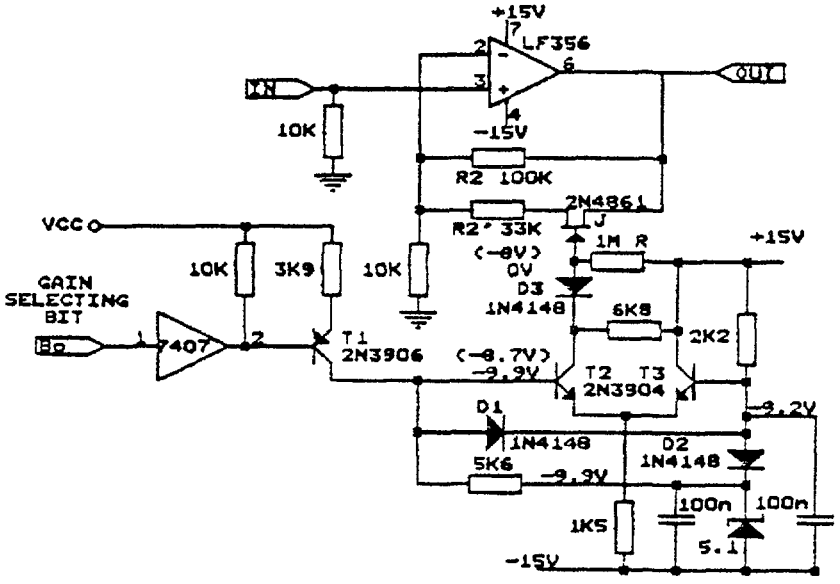


Fig. 2.13.1: Digitally preset amplifier gain circuit.

The gain selecting bit is applied to the input Bo.

Assume B_0 is at first at logic 0, B_0 = 0V.

The transistor T_1 will be ON, as the output of the logic driver SN 7407 is low and the collector current of T_1 flowing into diode D_1 keeps T_2 conducting and T_3 off. The collector current of T_2 flowing across the resistor R maintains J in the open-circuit condition. Therefore the feedback path around the operational amplifier consists of the 100 K resistor, connecting the output of the amplifier to its inverting input. and of a 10 K resistor from this input to ground. Neglecting the ON resistance of J, the system has a closed-loop gain of about 11.

Suppose now B_0 raised to logic 1. T_1 is turned off and along with T_1 also diode D_1 goes off. The transistor T_3 is now ON, and T_2 is OFF. As no collector current flows across R, the JFET J becomes a short circuit. The gain of the system, neglecting the ON resistance of the field-effect transistor is determined by the ratio:

$$1 + \frac{R_1 + \dfrac{R_2 \cdot R_2'}{R_2 + R_3'}}{R_1} \approx 2.5$$

EXPERIMENT

After assmbling the circuit shown in Fig. 2.13.1, check all the DC voltages you can read from the figure with $B_0 = 0$ V and with $B_0 = 5$ V. In a few points, two different values are indicated. The values in brackets correspond to $B_0 = 0$ (input B_0 is grounded).

If in both cases the values shown in the circuit are reproduced with an acceptable degree of tolerance, apply a signal of about 100 mV to the LF356 input (IN) and check the values of the gain, by setting the gain selecting bit to logic 0 and then to logic 1.

Now apply a DC level of 100 mV to the amplifier input (IN) and send a square wave signal swinging between +5 V and 0 V with frequency of 1 kHz. Look at the waveform at the amplifier OUTPUT, and verify that the output is a square wave periodically switching between 250 mV and 1.1V.

EXPERIMENT 2.14

LINEAR GATE WITH SATURATED TRANSISTOR

OBJECTIVE

A simple version of linear gates suitable for the single polarity pulses will be studied with respect to the speed and the residual voltage.

REVIEW

A linear gate with the saturated transistor is given in Fig. 2.14.1.

The transistor acts like a switch. When it is open the input signal appears at the output. With the switch closed, the output is grounded, and signal disappears. In practice, some residual voltage will exists across the transistor because of its finite resistivity in the conducting state. With the base grounded, the transistor is nonconducting . Conduction is ensured when the current will flow into the base.

In nuclear electronics, very fast gates are often required. There are limitations on the transistor switch-on and switch-off times.

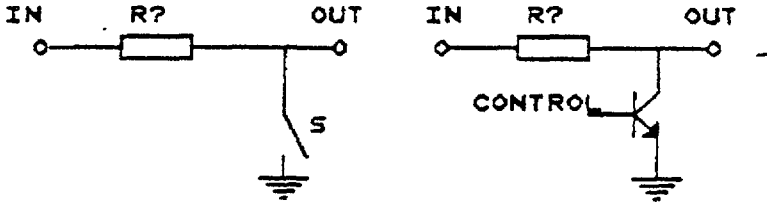


Fig. 2.14.1: Illustration of linear gate

When the transistor turns to the nonconductive state the collector-base capacitance C should be charged through the resistor R. In principle we can reduce the value of the resistor R to decrease the time constant RC. However, the residual voltage will be greater than with the bigger resistor R. Therefore, the only practical solution is to use fast switching transistors instead of the more usual signal transistors.

When the base current starts to flow, the decreasing current amplification factor beta for higher frequencies as well as its complex character limits the speed of the response.

A few tricks are introduced to optimize performances.

1. Instead of the transistor control voltage varying between zero and a few volts, you can take the voltage with the amplitude between 3.5V and -0.5V. Such voltage is provided by the fast comparators like the LM710, the LM311 and similar. Base of the transistor will be discharged faster if the negative voltage will be applied.

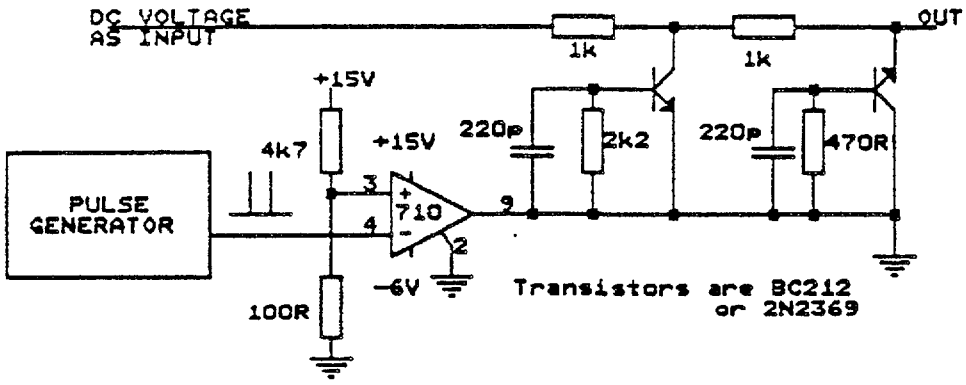
2. The transition can be accelerated if the base resistor is bypassed by an adequate capacitor.

3. The residual can be almost removed if two linear gates are connected serially. The second transistor is inverted; i.e the base and the emitter terminals are interchanged. Any transistor, pnp or npn, is in principle symmetrical. However, the base-collector pn region has lower carrier density to keep smaller electric field strength across, and make transistor suitable for higher voltage operation. In the inverse use, the current amplification factor β is much lower. To reach saturation, a much greater base current must be used.

All above tricks have been used in the design of the linear gate shown in Fig. 2.14.2.

Fig. 2.14.2:

Linear gate circuit.



EXPERIMENT

Assemble the circuit with the small signal transistor BC182 and the fast switching transistor 2N2369 and compare their characteristics. To see the switch-on and switch-off times, apply a constant voltage of 5 V at the input, and short pulses to the 710 comparator. Observe the output signal. Which are the shortest output pulses you can get at the output without any deterioration?

EXPERIMENT 2.15

TIME INTERVAL-TO-AMPLITUDE CONVERSION

OBJECTIVE

This experiment aims at showing how the linear conversion of a time interval into an amplitude proportional to it can be employed in the measurement of the time between two nuclear events.

REVIEW

Consider a time interval defined by two nuclear events. TIME-TO-AMPLITUDE conversion is the operation which transforms the time between the two events into an amplitude proportional to it. The amplitude is then converted into a number by an analog-to-digital converter. TIME INTERVAL-TO-AMPLITUDE conversion is therfore a preliminary step to a particular kind of TIME DIGITIZING. It is employed whenever the time interval to be digitized is so short and the resolution required so high that direct TIME INTERVAL-TO-DIGITAL CONVERSION is not feasible because of the very high clock frequency that would be needed. Besides that, TIME INTERVAL-TO-AMPLITUDE Conversion may be useful whenever an amplitude digitizing system is already available and therefore an analog interface between time intervals and signal amplitudes extends in the most straightforward way the digitizing function to the time variable.

In the following, the two nuclear events will be assumed to be interactions of nuclear radiations with detectors. The instant of occurrence of the two events is defined from the electrical pulses delivered by the detectors by suitable timing triggers.

It will be assumed that the output signals from the timing triggers are short pulses. Obviously they are delayed with respect to the true nuclear events, in the sense that the electronically defined time of occurrence of the event does not coincide with the actual time of an occurrence of the physical events. A pure delay, the same for both events, would be of no importance as the parameter of interest in nuclear experiments is the TIME DIFFERENCE between events, not their absolute position in time.

In the measurement of time intervals, the pulse which comes earlier is customarily referred to as the START SIGNAL, while the pulse which comes later is called the STOP SIGNAL.

Time interval-to-amplitude conversion is realised in the following way. Generation of a linear ramp begins as soon as the START SIGNAL is received. The linear ramp stops when the STOP SIGNAL comes in and the value reached is held for the time necessary for analog-to-digital conversion.

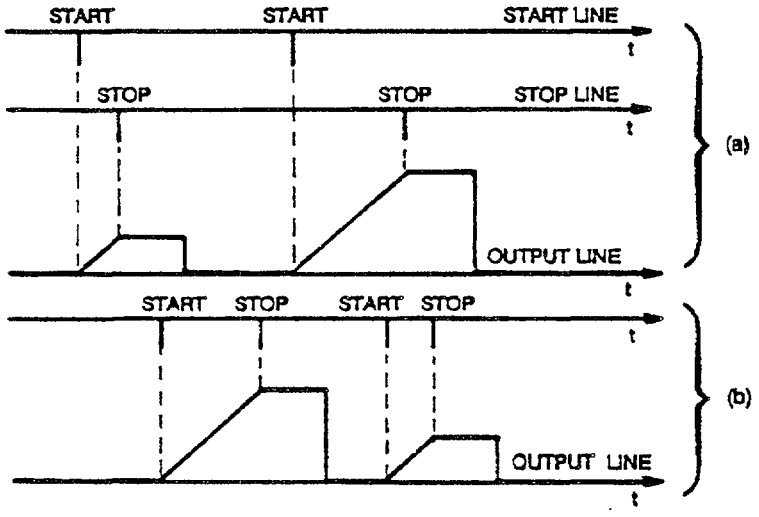
Depending on the particular experiment, START and STOP may appear on physically separate lines, as when come from timing triggers associated with two different detectors, or they may appear on the same line. The latter occurs, for instance, in the analysis of the probability distributions of time intervals between pairs of events generated in the

same detector. This is the case, for instance, in which the distribution of time intervals between events is monitored to determine whether ro not the distribution is Poissonian.

The principle of TIME INTERVAL-TO-AMPLITUDE CONVERSION is described by the timing diagrams of Fig. 2.15.1.

Fig. 2.15.1:

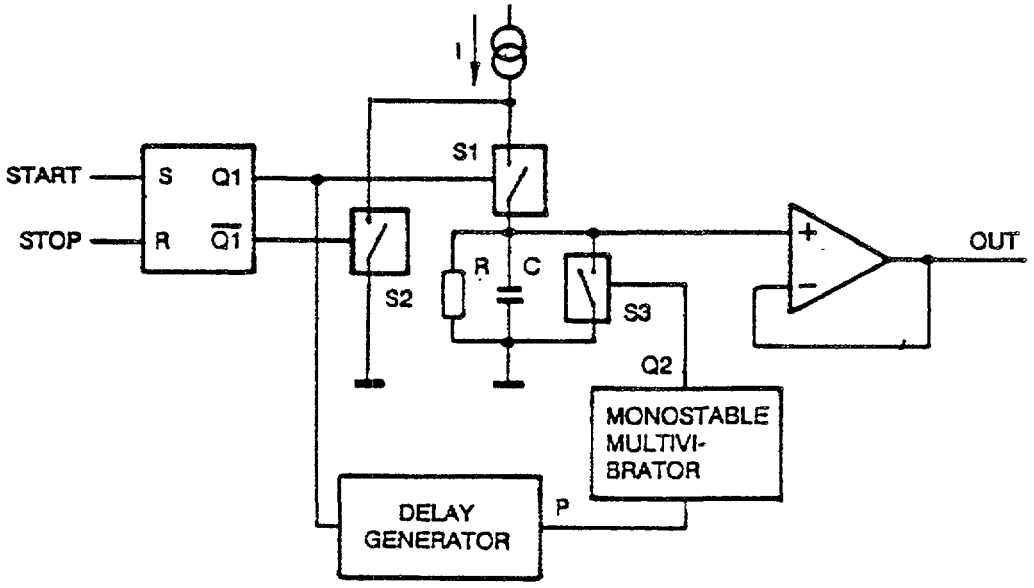
Principle of time to amplitude conversion.



The principle of TIME INTERVAL-TO-AMPLITUDE-CONVERSION is implemented by a circuit known as a TAC (time-to-amplitude converter). The simplified block diagram of a TAC intended for pulses appearing on separate lines is shown in Fig. 2.15.2.

Fig. 2.15.2:

Example of realization of a TAC



In the description of this circuit, as well as for other circuit analysis to be made it is conventional to assumed that the analog switches are closed when the control voltage V_L is at logic level HIGH and they are open when V_L is at logic level LOW.

Fig. 2.15.3 presents the timimg diagram for the circuit given in Fig. 2.15.2. Assume that before the arrival of the START pulse the flip-flop has Q_1 = LOW and Q_1 = HIGH and that accordingly S_1 is open and S_2 is closed.

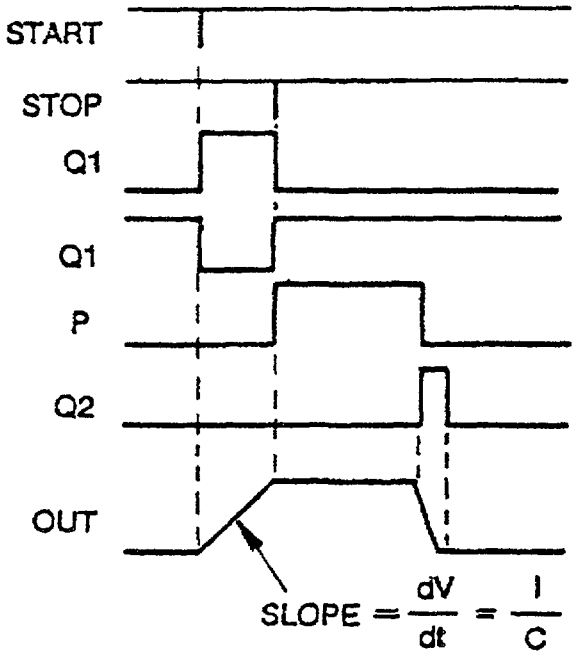


Fig. 2.15.3:

Timing diagram of TAC.

The monostable multivibrator in the initial state has the Q output at logic level LOW and therefore S_3 is open. Under these conditions the constant current source I is diverted to ground through S_2. The resistor R provides a DC path to ground for the leakage currents of the switches S_1 and S_3 and for the bias current out the output buffer, thereby preventing the voltage across the capacitor C from drifting indefinitely. The value of R must be large enough, 10 M or more, to avoid intolerable nonlinearity in the generation of of the linear ramp. If the sum of the leakage currents of S_1 and S_3 and the bias current of the output buffer do not exceed 10^{-10} A, which requires that the buffer has a field-effect transistor at the input, the voltage error across C would be less than 1 mV.

The dynamic behaviour of the circuit is as follows. The START pulse sets the Q output of the flip-flop to logic HIGH and the Q output to logic LOW thereby diverting the current I into the capacitor C. A voltage ramp is therefore generated across C. The linear charging of C stops when the flip-flop is reset by the STOP pulse. The voltage reached by the capacitor at the end of the time interval under measurement is temporarily held on C.

The HIGH-to-LOW transition in the flip-flop Q output initiates the following sequence. A time interval, equal to the desired holding time, is produced by in the delay generator. Once this characteristic delay has elapsed, the output signal from the delay generator triggers the monostable multivibrator, which at the output Q provides a short positive pulse. The function of this pulse is that of closing the switch S_3 thus restoring the voltage across C to zero. Once the monostable multivibrator recovers to the initial state, the TAC is ready to process a new time interval. The described principle can easily be transferred into that suitable for pairs of events on the same line by simply replacing the SET-RESET flip-flop configuration with a TOGGLE flip-flop.

It is worth pointing out that a real TAC is somewhat more complicated than the circuit diagram of Fig. 2.15.2 would imply. What makes it more complicated are the auxiliary logic functions that have to be added to prevent false operation. For instance, if a START signal is not followed by a STOP signal within a given time which corresponds to the instrument full range, the capacitor C must be automatically reset.

A STOP signal not preceded by a start signal must not activate the TAC.

Some more elaborate logic decisions may also be needed to improve the TAC rejection of ambiguous situations.

Circuit description

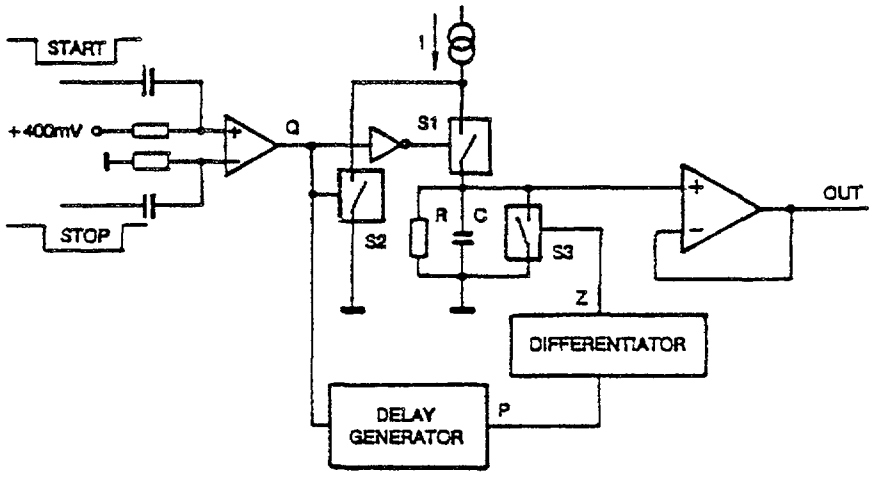
The input section of the TAC differs from the flip-flop structure outlined in Fig. 2.15.2 for two reasons. One is that to increase the versatility, an input configuration was chosen which not only enables the experimenter to convert into amplitude a TIME INTERVAL, but also the PULSEWIDTH. This circuit associated with a multichannel analyser, permits the width of a rectangular signal to be measured with high accuracy. The second reason why the classical approach based upon a flip-flop was abandoned is that in the configuration adopted here, the reset operations after a measurement are implemented in a much simpler way. The basic circuit diagram of the TAC is shown in Fig. 2.15.4.

The TAC requires that the START and STOP signals be negative pulses, 10 μs long, with a 0.5 V minimum amplitude. The circuit measures the TIME INTERVAL between the NEGATIVE GOING EDGES of start and stop signals. If the circuit has to be employed in a real experiment and the timing triggers, as was assumed so far, deliver very narrow pulses, these pulses must be reshaped by two monostable multivibrators with about 10 μs characteristic duration. For the planned laboratory exercise, this will not be necessary, as the tests will be made using one or two synchronized artificial pulse generators, whose widths can easily be adjusted to the required value.

The working principle of the circuit of Fig. 2.15.4 is as follows.

Fig. 2.15.4:

Basic circuit of the TAC.



The analog comparator has the non-inverting input biased at 400 mV, while the inverting input is connected to ground via a resistor.

The start and stop signals are applied to the non inverting and inverting input respectively, through decoupling capacitors of large value. In the initial state, therefore, the comparator output is at a logic level HIGH and this keeps S_1 open and S_2 closed. The switch S_3 is open in the initial state. The current I is diverted to ground and the voltage across C remains close to zero thanks to the resistor R in parallel.

When the START signal, larger that the treshold, about 500 mV, is received, the comparator switches. Its output drops to logic LOW with the effect of closing S_1 and opening S_2 while S_3 still remains open. The current I is steered into C and the linear ramp is generated. See Fig. 2.15.5 for corresponding waveforms.

When the STOP signal is applied at the inverting input the original condition in which the non inverting input of the comparator was at a higher voltage than the inverting one is restored. The comparator output switches back to logic HIGH, S_1 opens and S_2 closes. The current I gets diverted to ground again and C remains charged at the voltage reached when the NEGATIVE GOING EDGE of the STOP SIGNAL was applied.

The delay generator is activated by the LOW-TO-HIGH transition in the comparator output. At the end of the delay interval, a short positive pulse shaped by the differentiator closes S_3 and this resets the charge on the capacitor. The voltage across C is taken by a low input current buffer and made available at low impedance for further processing.

The circuit of Fig.2.15.4 differs from that of Fig. 2.15.2 in that the structure of the input section employs a comparator rather than a flip-flop. Other differences are of minor importance. The linear ramp generation, the capacitor reset, and the output signal buffering are identical in both circuits of Figs. 2.15.2 and 2.15.4.

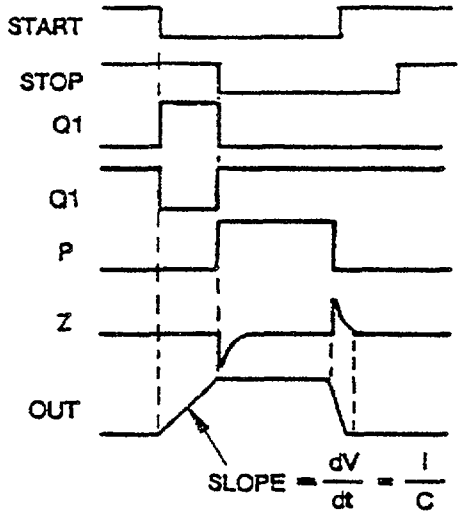


Fig. 2.15.5: Timing diagram of a TAC.

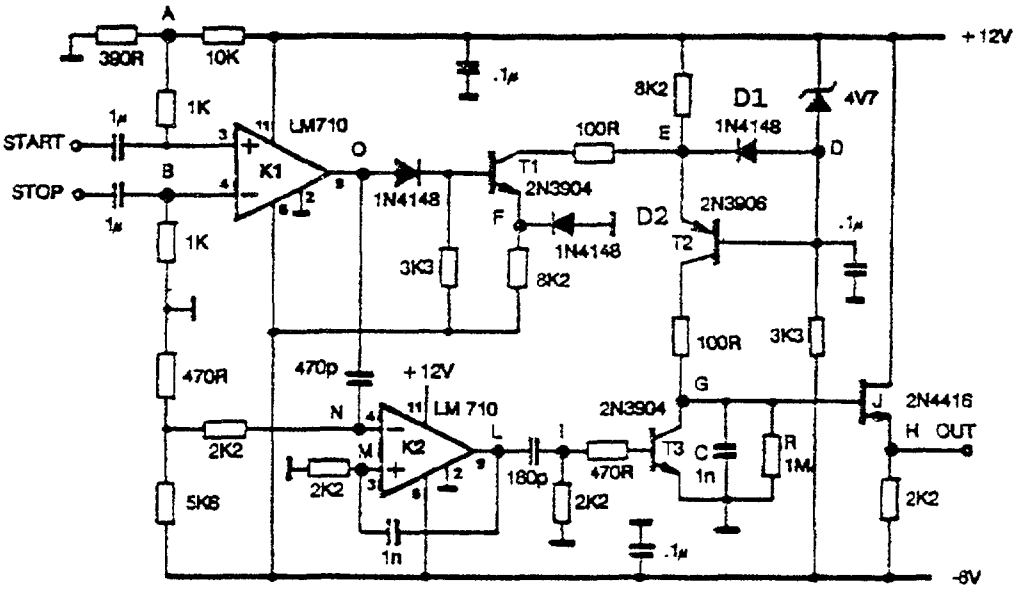


Fig. 2.15.6: Detailed circuit diagram.

Note: Pin assignement of LM710
for LM710N or LM710CN (Dual in line package)

The use of a comparator at the input extends the application of the circuit to the case in which the width of a pulse, rather than the time interval between pulses, has to be converted into an equivalent amplitude. The pulse whose width has to be measured must be sent to the START input and no signal must be sent to the STOP input.

The detailed circuit diagram of the TAC is shown in Fig.2.15. 6. The input comparator is realized with the monolithic circuit K_1 (LM710). The second LM710, labelled K_2 implements the delay generator.

Transistor T_2 is the constant current generator and S_1, S_2, S_3 control its state, enabling or disabling the generation of the linear ramp.

C is the capacitor across which the linear ramp develops when the collector current T_2 is turned ON. The transistor T_3 implements the function of a reset switch. The initial condition of the circuit of Fig. 2.15.6 is the following one.

The output of K_1 is at logic HIGH, therefore the voltage at node 0 is about +3V.

Transistor T_1 is ON.
The voltage at node F is about 2.3 V.
The diode D_2 is reverse biased.
The collector current of T_1 is 1 mA.

This current cannot be entirely supplied by the 8.2 K resistor connected between the node E and the positive supply voltage. Therefore the diode D_1 must be ON. The transistor T_2 is OFF; the node E is at about 6.6 V. The current balance at node E gives:

$$I_{T_1} = \frac{12 - 4.7\,V_E}{8.2} + I_p \qquad \text{(all the currents expressed in mA).}$$

As previously said, V_E = 6.6 V. Therefore I_p = 450 μA. The voltage at node N is about -0.5 V, therefore the voltage at node L is around +3 V. The voltage at node I is 0 V and transistor T_3 is OFF. The voltage at node H, the output voltage is slightly positive. Dynamically the circuit works in the following way.

The START signal, which must be of a negative polarity, with an amplitude exceeding 0.5 V and a width larger than 10 μs switches K_1. The output jumps to a slight negative voltage, about 500 mV in magnitude. As a consequence T_1 is turned OFF, because its emitter is clamped to -700 mV by the diode S_2. Diode S_2 becomes reverse biased and T_2 is turned ON. The emitter current of T_2 is given by:

$$\frac{12\,V - (12\,V - 4.7\,V) - V_{BE}}{8.2} = 0.5\ mA$$

This current, flowing into C charges it linearly. A voltage ramp appears at the output.

The HIGH-TO-LOW step which appears at node 0 is transmitted as a negative short spike to the inverting input of K_2 by the 47 pF differentiating capacitor. This spike has no effect, for it goes on the already negative non inverting input.

Suppose that now the STOP signal, again negative in polarity, more than 0.5 V in amplitude and more that 10 μs in width is applied at the appropriate input. The comparator output quickly switches to the logic HIGH back again. T_1 is turned ON, P conducts and T_2 goes OFF.

The collector current of T_2 stops flowing and C remains charged at the voltage close to the one stored when the STOP signal was applied.

The spike induced at the inverting input of K_2 by the LOW-TO-HIGH step at node 0 differentiated by the 47 pF capacitor triggers the comparator K_2, which is connected as a monostable multivibrator. A negative rectangular signal, about 3.5 V in amplitude appears at node L, which is transmitted differentiated to node I. The negative spike at I has no effect. The positive one drives T_3 into heavy conduction, thus discharging C until T_3 saturates and the voltage across C is reset to zero. As soon as the driving positive spike on the base of T_3 is over, the circuit is ready for a new operation.

The approximate value of standing voltages and currents are summarized in Table 2.15.1.

TABLE 2.15.1.

NODE	VOLTAGE	NODE	VOLTAGE
A	400 mV	H	+1 V
B	0	I	0
D	7.3 V	V	+3 V
E	6.4 V	M	0
F	1.8 V	N	-500 mV
G	0	O	+3 V

Branch	Current
T1 Collector	1 mA
T2 Collector	0
J Drain	3 mA

Construct the circuit of Fig. 2.15.6 on the available printed circuit board. The components layout is given in Fig. 2.15.7.

EXPERIMENT

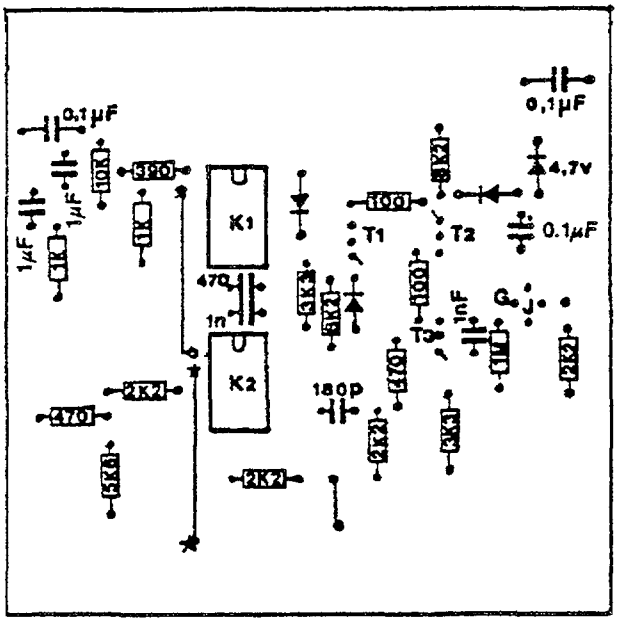
Once the circuit is ready, check it carefully before connecting the power supplies.

Connect the power supplies, check all the DC voltages and make sure that within reasonable inaccuracies due to components' tolerances, they reproduce the values of Table E.1.

- Send a negative signal with an amplitude of 0.5 V and a width of 10 μs to the STOP input. Nothing must happen in the circuit.

Fig. 2.15.7:

Components layout for TAC.



- Send the same signal to the START input. The trapezoidal signal, with a linearly rising part at the beginning followed by a flat top and then by a quick recovery to zero must appear at the output.

Check the slope in the linearly rising portion. It must be about 0.5 V μs.

Reduce the duration of the START signal and observe that the final amplitude of the output signal, node H, must be reduced accordingly.

If everything works correctly, check the linearity of the TAC by sending to the START input ten different values of the START PULSE width. The values of pulse width recommended are:

1μs, 2 us, 3 μs, 4 μs, 5 μs, 6 μs, 7 μs, 8 μs, 9 μs, 10 μs.

Measure these widths with the highest possible accuracy using the 1 μs/div time scale of the scope. Measure with the scope the final amplitude of the pulse at node H. Plot the output amplitude as a function of the START signal. The resulting diagram should be linear.

Having tested the TAC in the PULSE WIDTH measuring mode, you can test it now in the TIME INTERVAL MEASURING MODE.

For this application, use two generators synchronized in the way shown in Fig. 2.15.9. to obtain start and stop pulses and connect them to the appropriate inputs in the circuit.

Check with the scope the waveforms at points 0, E, N, I, H and make sure that they correspond to the ones sketched in Fig. 2.15.8. Test the linearity again using the previousiy explained method.

Once linearity has been checked, calibrate your TAC by using the delay lines of accurately known delays, and a single pulse generator, according to the diagram of Fig. 2.15.10. As the TAC has already been checked for linearity, two values of delays will suffice for the calibration. Represent on a linear scale the channel numbers corresponding to the two values of delay. Join the two points, obtained in this way, by a straight line. This gives the calibration curve of the TAC.

Go back again to the two synchronized generators of Fig. 2.15.9, fix a value of delay between start and stop around about 3 μs and measure it accurately using the MCA and the previously obtained calibration curve.

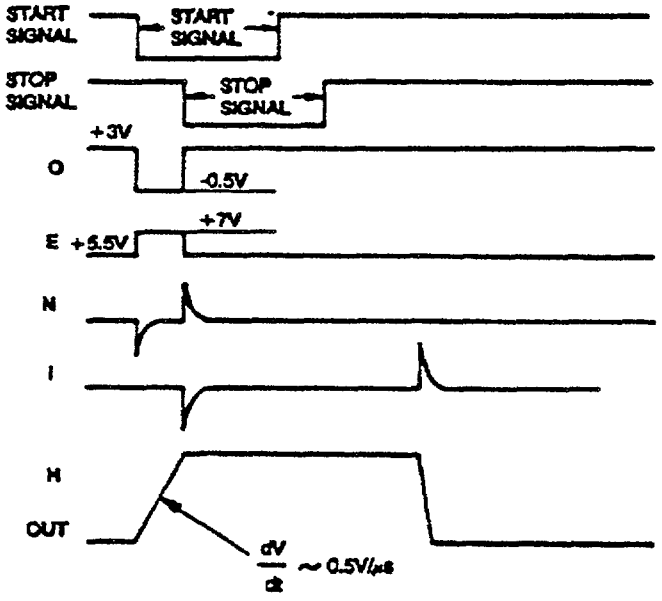


Fig. 2.15.8: Waveforms

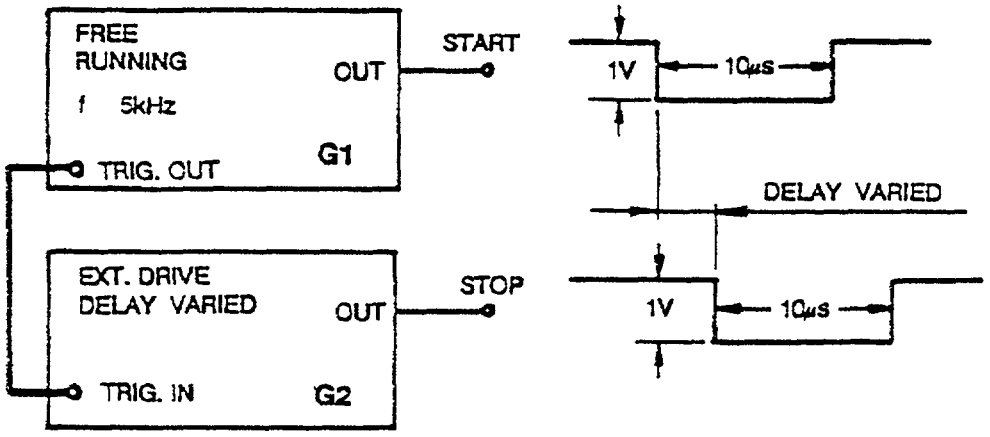


Fig. 2.15.9: Connection of two generators to obtain START and STOP pulses.

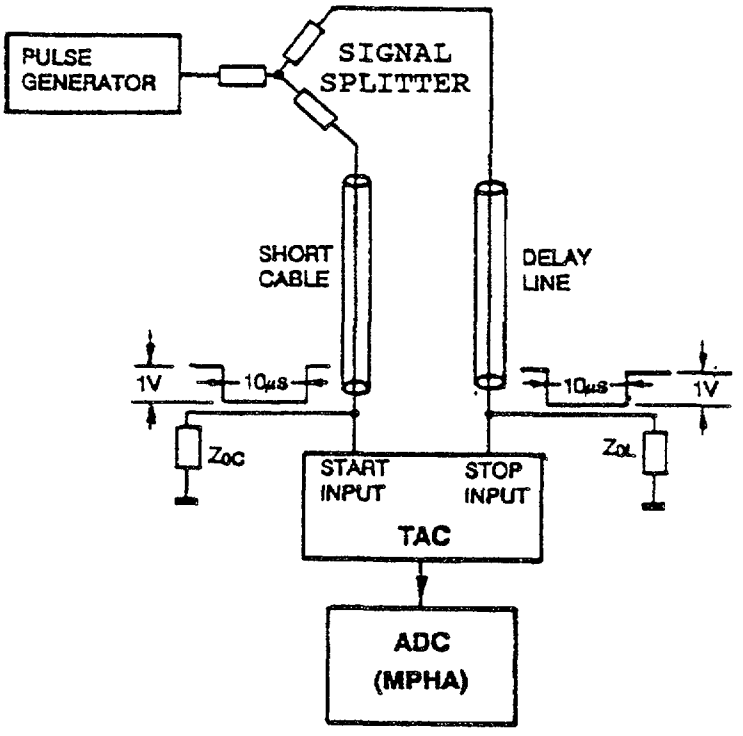


Fig. 2.15.10:

TAC calibration with delay lines and MCA.

EXPERIMENT 2.16

COAXIAL CABLES AND DELAY LINES

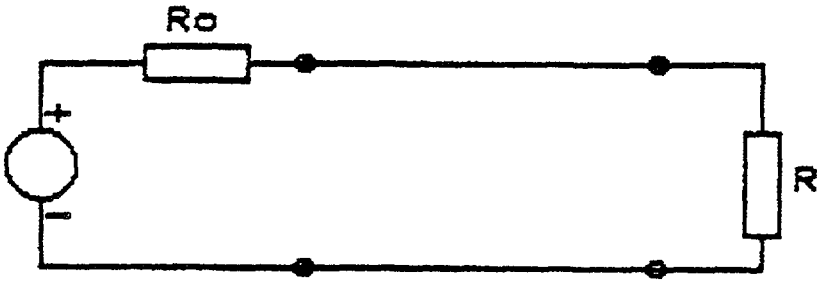
OBJECTIVE

The objective of this experiment is to discuss characteristic parameters of coaxial cables and delay line.

REVIEW

Coaxial cables are the transmission lines normally used in the interconnection of nuclear modules. Like any other transmission line, they exhibit inductance and capacitance per unit length which together determine the characteristic impedance of the line. This is the impedance the generator sees while the signal is travelling along the line.

Fig. 2.16.1: Transmission line.



If the load impedance at the load end of the cable does not have the same value as the characteristic impedance, a portion of the voltage and current travelling along the cable toward the load will be reflected at the load, resulting in signals travelling back towards the generator end of the cable. The output impedance of the generator should also have the same value as the cable impedance if any reflection coming from an imperfect impedance match at the receiving end is to be absorbed. These properies are briefly discussed below.

Assume that the transmission line is made of two parallel wires of lenght l , and that a voltage generator of output impedance R_0 is connected through it to a load resistor, as the diagram of Fig. 2.16.1 indicates. The line has both a capacitance C per unit lenght, and an impedance L per unit lenght. Suppose that at time t = 0 the generator produces a voltage step of amplitude V. According to the laws of electromagnetism, this voltage step will travel along the line with a velocity $u = \frac{1}{\sqrt{LC}}$. When this voltage front moves by a distance dx, a capacitance Cdx has to be charged up to the voltage V. This requires a charge dQ = C dx V, to be suppplied by the generator during the interval dt, i.e. the

time that the voltage front takes to move over a distance dx. While the step propagates along the line, the generator is supplying a current

$$I = \frac{dQ}{dt} = C V \frac{dx}{dt} = C V u = V \sqrt{C/L} = \frac{V}{Z}.$$

The quantity $Z = \sqrt{L/C}$ is called the characteristic impedance of the line. It is a real number, measured in ohms. It represents the ratio between the generator voltage and the current it supplies while the step is travelling down the line. If the line is terminated with a resistor R = Z, the generator will continue to supply the same current when the step arrives there; therefore, the generator can not tell the difference between a line terminated with its characteristic impedance (Z) and an infinite line.

Suppose that the line is short circuited (R = 0). At the end of the line, the short requires that the voltage be zero. Wave theory indicates that an easy way to establish these boundary conditions is to consider the signal on the transmission line to consist of an incident wave (travelling away from the generator), plus a reflected wave (travelling toward the generator). In the case under discussion, if the latter wave is a step function of amplitude −V, the zero voltage condition at the end can be met. This −V step function will travel back to the generator where it will reduce the voltage at the generator terminal to zero. If the generator is matched to the line, so that no further reflections occur, this step function has been transformed into a pulse by the properties of the transmission line. A little consideration of the problem will show that the pulse has a width of 2τ, where τ is the time necessary for the original step to travel the lenght of the line. In nuclear electronics, it is usual to call this process transmission line differentiation.

The other extreme situation is to have the end of transmission line open (R = ∞). The current at the end must now be zero. This condition can be met by means of a reflected current step of the opposite sign of the incident current step. In a time τ, the reflected current step will arrive back at the generator where it will produce a voltage step equal to the original step (the generator is mached to the line). Thus the signal at the generator will look like a step in which another step of the same amplitude, but delayed by the time 2τ, has been superimposed.

In signal transmission, the reflections are to be avoided and therefore all the transmission lines are to be terminated in their characteristic impedances.

In nuclear electronics we find examples of transmission lines in the guise of coaxial cables, delay lines, and twisted wires. The twisted wires are typically used inside pieces of equipment. Delay lines are used to delay a signal by significant amounts, typically longer that 100 ns. This is equivalent of about 20 m of a coaxial cable. They usually consist of wires wound around a magnetic material, together with capacitors distributed across them. Characteristic impedances of about 1K are common. You can find delay lines in amplifiers (for shaping purposes, or just to delay signals), or in constant fraction timing single channel analyzers. For very short delays, coaxial cables are used.

In the followong, we refer to the coaxial cables, and describe the characteristics of some commonly used ones. They are used everywhere in the interconnection of modules. For fast logic signals, 50 R cable is used, and should always be properly terminated.

In many cases it is recommended that 93 R coaxial cables are used for analog signals. The higher impedance of these cables demands less current from amplifiers thus increasing system linearity. For short cable lengths impedance matching termination is not required as reflections are short enough not to cause trouble. Here short stands for lengths such that the transmission time is much smaller than the signal rise time. (For

example, a 1m cable gives negligible reflection with a 50 ns rise time signal; for most analog signal cables under 2m do not require termination.) For long lengths of 93 R coaxial cable, 91 R or 100 R (standard resistance values) provide adequate termination.

In the case of linear outputs, nuclear modules usually provide two connectors, one giving the signal through low source impedance and the other through 93 R. The low impedance output is normally used for short lengh connection but if the cable is long and not terminated, reflections and/or oscillation can occur. In this case the 93 R output should be used.

The cable capacitance is also an important parameter to be considered in some cases where the cable is unterminated, such as in detector-preamplifier interconnection. To reduce noise, low capacitance at the preamplifier input is required. The capacitance per unit length is inversely proportional to the ratio of conductor diameters and directly proportional to the dielectric constant of the material between conductors. The characteristic inductance is determined by the same factors. Thus similarly constructed cables with the same impedance will have the same capacitance per unit length, regardless of the diameter size. Because of their lower capacitance, 100 R cables are recommended for detector preamplifier connections.

A comparison of coaxial cables is give in Table 2.16.1. below.

Table 2.16.1: Properties of selected coaxial cables

Cable Type	Impedance (ohm)	Capacity/Foot (pF)	Outside Diam. (in.)	Matching Connector
RG-58C/U	50	29.5	0.199	UG-88/U(BNC)
RG-59A/U	75	20.5	0.242	UG-260/U(BNC)
RG-62A/U	93	13.5	0.249	UG-260/U(BNC)
Microdot 93-3913	100	13.0	0.132	Microdot 32-75

The current capability of the output stage should be checked when a cable is terminated; for example a current of 100 mA must be supplied to develop a 10V signal in a 100 R terminated cable. Of couse, while the signal is travelling along the cable, the generator sees an impedance equal to the cable impedance.

Perform the experiments following the instructions given below.

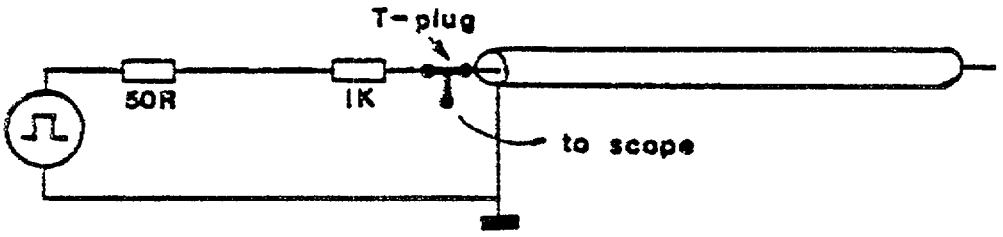
EXPERIMENT

1. Mount a BNC plug to one end of the cable.

2. Connect a 1K resistor to the output of the pulse generator to increase its output resistance (normallyl 50 R) as shown in Fig. 2.16.2. Solder a cable to the resistor and make sure that the ground connection to the output connector is as short as possible.

Fig. 2.16.2:

Cable capacitance measurements.



Apply a pulse (for example,. 5V, 10 ms) to the cable. Connect the probe of the oscilloscope to the input of the cable and measure the rise time of the pulse. Calculate the capacitance C of the cable per unit length (pF/m).

3. Connect a coaxial cable (length ≈ 6m) to the pulse generator via a BNC-T piece (see Fig. 2.16.3). Check the pulse shape at the cable input (use the probe):

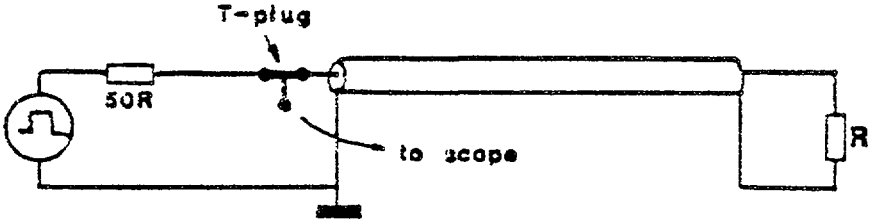
a) with the cable open at the far end (R = ∞),

b) with the cable shorted (R = 0)

c) with a 1K potentiometer at the end, adjusted to to match the impedance.

Fig. 2.16.3:

Measurements of reflections.



Measure the transmission delay time τ of the cable (ns/m). Calculate the inductance L (μH/m) and the characteristic impedance from the relations and compare the latter with the value obtained from the impedance matching.

$$\tau = \sqrt{L\,C}$$

$$Z = \sqrt{L/C}$$

d) Observe multiple reflections (at the receiving and sending ends) by repeating a) and b) with a resistor (220 R) in series with the generator output.

4. Delay lines behave like coaxial cables but with much larger values of τ and Z_0 (this is due to a comparatively larger value of L). Repeat problem 3 above with a 1 ms delay line (if necessary place a resistor in series with the potentiometer so that matching may be achieved.

5. Make a twisted pair of a few meters lenght and repeat problem 3. You may see that within reasonable limits, the characteristic impedance is not sensitive to the way you twist the wired, or to the type of wires used.

PART THREE

DIGITAL CIRCUITS

Digital circuits - an introduction.

Digital circuits are present practically everywhere in nuclear electronics, from amplifiers to MCAs. The available digital components include a wide range of devices, from simple small scale integration combinational and sequential elements, such as gates and flip-flops, to large scale integration counters and microprocessors. User programmable ICs are nowadays also a common component in many designs.

Part of the designer's effort is related to the logic function and structure of the circuits they design,independently of the technology on which the circuits are to be implemented. Another part of their effort is related to the electrical and timing characteristics of the ICs that are to be used. Likewise, maintenance engineers must be familiar with the principles and techniques of digital electronics if they are to be successful in a field where instruments are subject to continuous technological evolution.

The present part of this Manual deals with digital electronics. It offers a guided tour of the logic catalog and suggests many experiments to help in the correct understanding of the logic function and electrical properties of the components. A short, practical review of the standard techniques for the logic design of combinational and sequential circuits is given. The importance of both hardware and software tools is emphasized by describing some of them in separate experiments.

EXPERIMENT 3.1

STANDARD INPUT CHARACTERISTICS AND INTERFACING OF LOGIC GATES

OBJECTIVE

The objective of this experiment is to present the characteristics of two of the most widely used logic families, to understand their driving requirements and capabilities, to practice on interfacing logic families to one another and to other circuits.

REVIEW

In this experiment we will only refer to CMOS and TTL families. The many subfamilies of both the CMOS and the TTL groups differ significantly in their driving requirements and capabilities; we will deal with the TTL low-power Schottky, usually designated as the LS subfamily, and with the HC and CD subfamilies of CMOS.

TTL is important as a family because of the very broad range of available integrated circuits. It is still the dominant family in the small and medium scale integration range of circuits, but is being overtaken by CMOS circuits. These have the advantage of an extremely small power dissipation in the quiescent state, and the latest circuits are practically as fast as the faster TTL circuits.

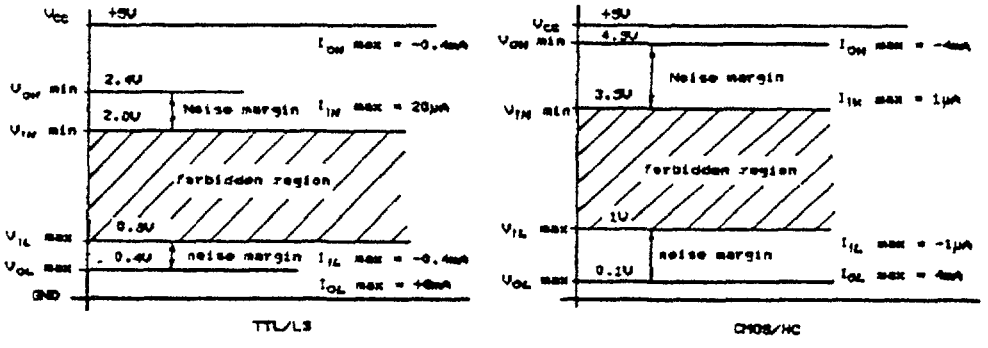


Fig. 3.1.1: Legal values for TTL/LS and CMOS/HC

Correct use of TTL and CMOS families requires a knowledge not only of their characteristic logic voltage levels and corresponding legal limits, but also of the driving requirements and output current capabilities. In practice, this is especially important when interfaces between the families or connectionSsto other circuits are required. Following tradition, we selected a NAND gate (74LS00) to represent the TTL family, and a NOR gate (74HC02 or CD 400l) to fly the CMOS colours. For reference, the legal voltage levels for TTL and CMOS powered at 5V are given in Fig. 3.1.1; also indicated are typical maximum values of guaranteed currents that still keep the voltages within legal

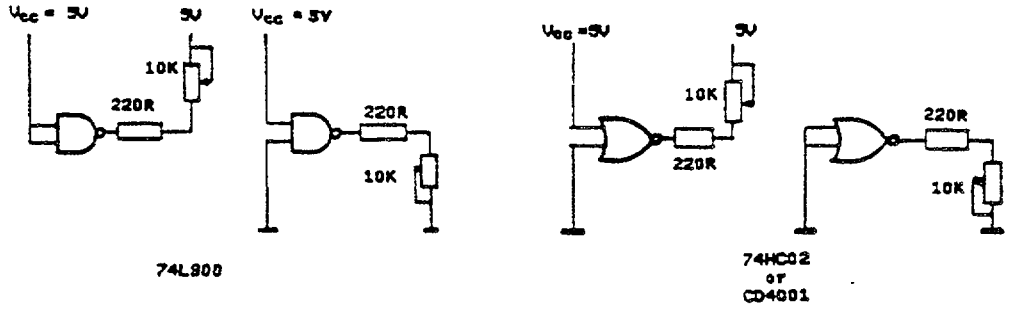
limits. (Note that the CD series has a much smaller output current capability than the HC series).

EXPERIMENT

Output current capability. The circuits of Fig. 3.1.2 can be used to obtain the output volt-ampere characteristics. The voltage is to be measured at the gate output; the output current is obtained through the voltage drop across the 220R resistor. Plot the voltage - current characteristics for both logic states.

Fig. 3.1.2:

Measuring output characteristics



You may have concluded that the values given in Fig. 3.1.1 are very conservative (actually, those values were arrived at assuming worst case conditions). You may apply the above results to show that the proper way of connecting an LED to a TTL/LS circuit is as shown in Fig. 3.1.3; the LED will be ON when the output state is 0. Resistor R is to be chosen to limit the current to the appropriate level; if the voltage drop in the diode is 2V, then a 330R resistor may be used ($I_o = 9mA$). Likewise, a small relay, switching with a current of a few mA, may be directly actuated by a TTL circuit if the driving current flows with output low as in Fig. 3.1.4. The role of the suppressor diode should be understood: it is necessary to limit the induced voltage at the relay terminal connected to the gate when the current stops.

Fig. 3.1.3:

Interfacing LED to an LS/TTL circuit.

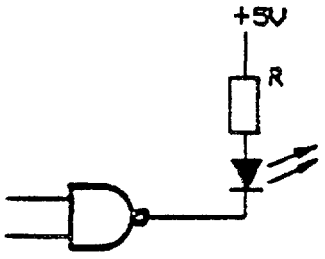
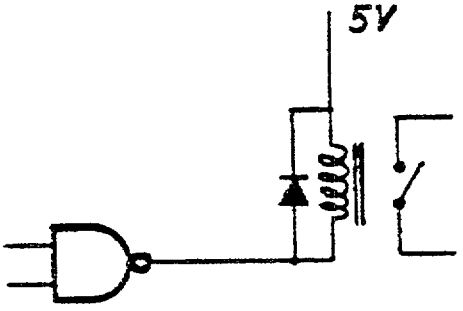


Fig. 3.1.4:

Interfacing a relay to a TTL/LS circuit.



Input characteristics. The input/output voltage transfer characterstic and the input current can be measured using the circuits shown in Fig. 3.1.5. Feedback forces the inverting input voltage of the operational amplifier to follow the voltage imposed on the non-inverting input by the 10K potentiometer irrespective of the current that flows out of or into the logic gate. By changing the potentiometer setting in steps of 0.5V, determine:

(i) the gate input to output transfer characteristic by measuring the voltage at points A and Y;

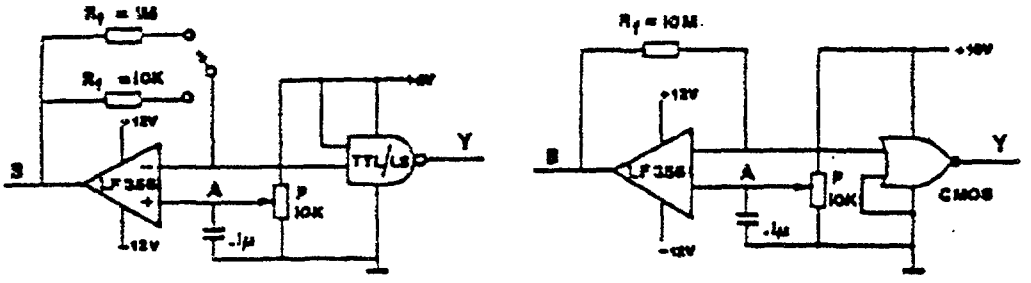


Fig. 3.1.5: Measuring input characteristics

(ii) the gate input characteristic by measuring the voltage at points A and B (the input current is given by $(V_B - V_A)/R_f$). The value of the feedback resistor R should be chosen to provide good sensitivity in the determination of the input current while keeping the operational amplifier out of saturation.

The measured values should indicate that one gate output is able to source or sink a current much larger than that needed at the input of another gate. The number of gates that can be driven from a single output is indicated in the catalog under the name of the fan-out; typical values are 20 for TTL/LS. For CMOS the input currents in either logic state are so low that, in practice, fan-out is limited by dynamic considerations as discussed in a later experiment.

TTL/CMOS family interfacing. The characteristics for TTL and CMOS gates show that if the two families are used together some care must be exercised in their interconnection. If both families use the same V_{cc} then in the TTL to CMOS connection it is necessary to use a pull-up resistor to obtain the legal level for state I at the CMOS input; and in the CMOS to TTL connection a transistor is used to assure compatibility for state O at the TTL input (this is a very conservative approach for the newest CMOS subfamilies like the HC); the value of R must be compatible with the maximum current that may be sourced by the CMOS gate. This is summarized in Fig. 3.1.6.

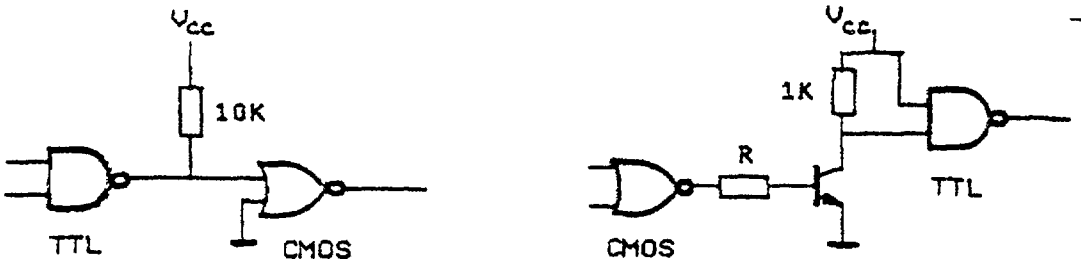
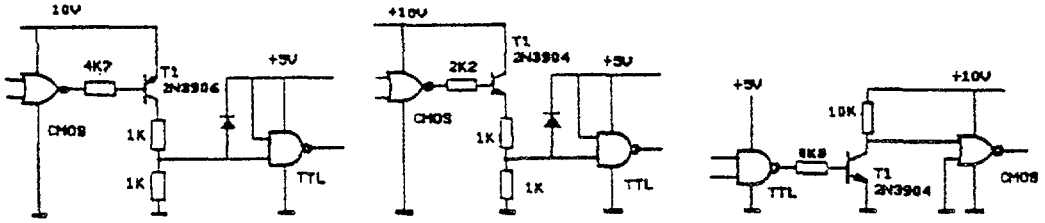


Fig. 3.1.6: Interfacing TTL- CMOS (using the same V_{cc} supply)

Whenever different values of the supply voltage are used for TTL and CMOS, level shifting is required. Interface examples are shown in Fig. 3.1.7. You may assemble the circuits and verify both the non-inverting and the inverting interface from CMOS to TTL and the (inverting) interface from TTL to CMOS. The resistors in the CMOS to TTL circuits have been chosen to allow any supply voltage above +5V to be used for CMOS; the diode clamps the voltage at the TTL input to a safe level near V_{cc}.

Fig. 3.1.7:

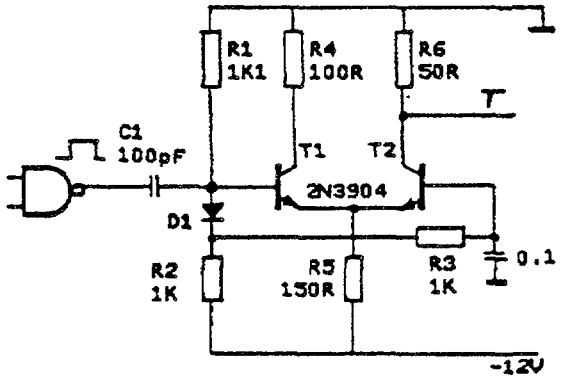
Interfacing TTL-CMOS (different Vcc supplies.



TTL to negative NIM logic interfacing. Conversion from TTL levels to fast NIM logic levels may be accomplished with the circuit shown in Fig. 3.1.8. Normally, T_1 is conducting and T_2 is cut off because the base of T_1 is one diode drop above that of T_2. A 1 → 0 transition at the TTL output is differentiated with a time constant $C_1 \times R$ where R is essentially the equivalent to the parallel of R_1, R_2 and R_3 (~35ns), and cuts T_1 off for a short period, thereby switching the current through R_5 to T_2. Thus the circuit is able to sink about 18mA from a 50R load, as required by the NIM fast logic standard. Assemble the circuit in Fig. 3.1.8 and measure its output impedance and the rise time for a load resistance of 50R.

Fig. 3.1.8:

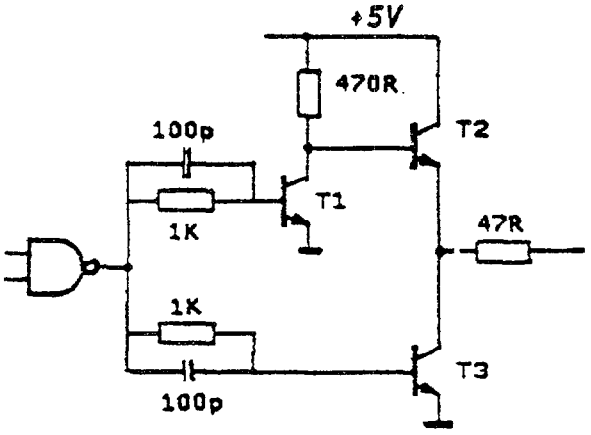
Interfacing to NIM negative logic



Increasing output current capability. Sometimes it is necessary to increase the output current capability of the gate. This is frequently done by using bipolar transistors, Darlington arrays or FETs, either as discrete components or in integrated form.

Fig. 3.1.9:

Interfacing to a 50 ohm cable.



As an example let us consider cable driving. The usual cable has 50 ohm impedance and enough current must be supplied to maintain the appropriate voltage levels while the signals travel along the cable. Also, the output impedance of the source must be close to 50 ohms to avoid cable reflections. The circuit of Fig. 3.1.9 is appropriate for this purpose. The speed up capacitors assure fast transitions at the output; the 47 ohm resistor (together with the very low output resistance of the conducting transistor, either T2 or T3) matches the cable impedance.

EXPERIMENT 3.2

SPECIAL INPUTS AND OUTPUTS OF LOGIC GATES

OBJECTIVE

The objective of this experiment is to present the characteristics of Schmitt trigger input and open collector and tri-state output stages of logic gates, to understand WIRED-OR connections and to introduce transceivers.

REVIEW

There is a narrow input voltage region where the logic gates behave as linear, non-saturated circuits. Circuit noise, especially for slow varying input signals, may cause false triggering of the gate; also the output signal has rise and fall times comparable to the time the input signal takes to cross through the linear region. A special input circuit is required for gates subjected to these conditions; such improved gates are referred to as Schmitt trigger gates because the input circuit is a *Schmitt type discriminator. This discriminator uses positive feedback to increase the gain,* and to speed up the switching, as well as to provide different triggering levels for positive-going and for negative-going signals.

Output stages that can be physically connected to each other are needed whenever signals from different gates are used to drive the same line. Two different solutions to this problem have been implemented; the corresponding output stages are usually referred to as open collector or tri-state. The WIRED-OR connection is a valuable application of open collector stages. Transceivers are essentially an application of tri-state stages; they are useful circuits in which the pins may serve as input or output.

EXPERIMENT

Schmitt trigger input. A circuit similar to that in Fig. 3.2.1 may be used to determine the Schmitt characteristics of such units as the hex Schmitt trigger inverter (74xx14, either of the TTL or CMOS type).

The input-output voltage transfer curve can be directly displayed on an oscilloscope in a setup as shown in Fig. 3.2.1. The input generator should deliver a triangular or sinusoidal waveform from 0V to 5V; if this waveform cannot be made always positive, a resistor-diode combination should be used, as shown in Fig. 3.2.1 to protect the gate input. You should be able to observe the hysteresis curve; in most circuits, the transition takes place at about 1.6V when the input signal is positive going, and at about 0.8V when it is negative-going.

You should also observe the output transition time when the input is a slowly varying signal. Together with the hysteresis, the increased speed due to positive feedback allows us to obtain, for example, reliable time marks from the electric supply network, with a circuit as simple as the one indicated in Fig. 3.2.2. For the same reason, Smidt gates are used to generate clean signals for initialization purposes in sequential circuits (that is, to reset or to set laches and flip flops at power-up) as is also indicated in Fig. 3.2.2.

Fig. 3.2.1:

Pertinent to the Schmitt trigger.

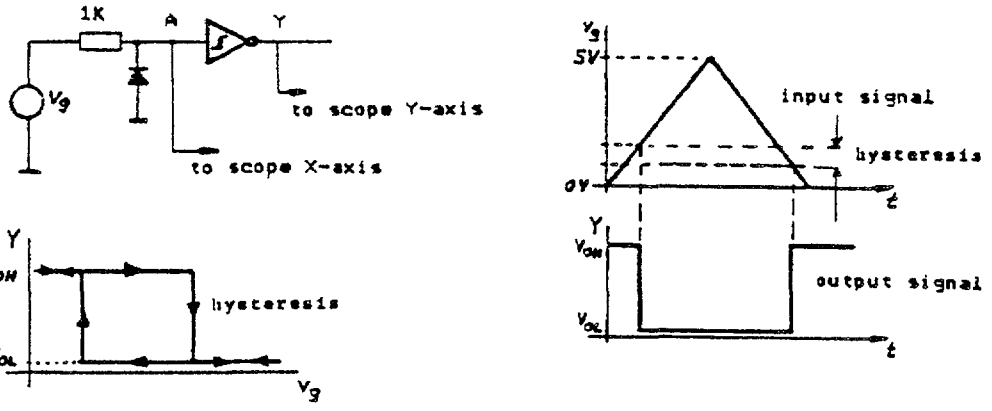
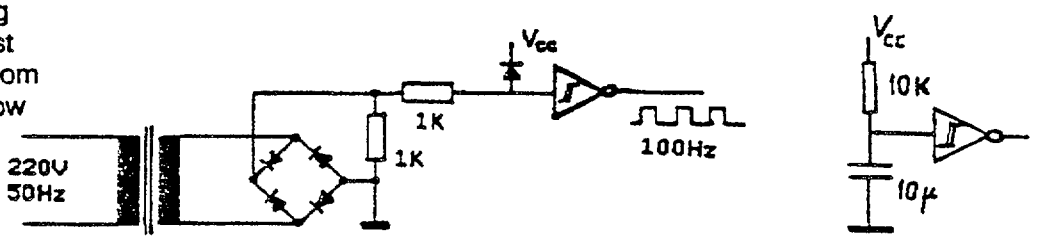


Fig. 3.2.2:

Obtaining clean, fast signals from noisy, slow ones.



Open collector output. A typical open collector gate is the 74xx03, a two-input NAND gate. The output stage consists of a single transistor, with the emitter connected to ground. The collector is not internally connected, it is just tied to the output pin. Therefore, an open collector output can sink, but cannot source current. The output sink characteristics can be measured using the appropriate circuit of Fig. 3.2.3.

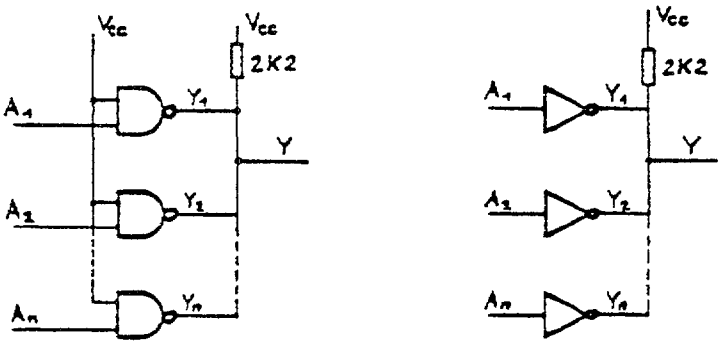
In practice, open collector gates are connected to a line with a single pull-up resistor, as shown in Fig. 3.2.3. The resistor assures that the line is always in a well defined logic state. This state will be zero (Y = 0) if at least one of the gate outputs Y_i is in state zero, that is

$$Y = Y_1\ Y_2 \cdots Y_n = \overline{A}_1\,\overline{A}_2 \cdots \overline{A}_n = \overline{A_1 + A_2 + \cdots + A_n}$$

Because of this equality, the connection is known as the WIRED-OR (the function implemented is actually WIRED-NOR). Note: the above expression is valid for the NAND gate circuit because a single input is used in each gate, the other being in logic state 1. A different function would be obtained if both inputs were used. Actually, in Fig. 3.2.3, the NAND gate is being used as an open collector inverter.

Fig. 3.2.3:

WIRED–OR connection



Open collector gates are frequently used to make connections to buses, as shown in Fig. 3.2.4 for a two-line bus. It can be verified that when the control variable C_i is in the low state ($C_i = 0$), the associated gates are effectively disconnected from the bus because the open collector has a very high impedance. In this application, not more than one of the control variables is supposed to be in state 1 at any one time. The bus lines will then be at 0 (imposed by the gate output transistor), or at 1 (imposed by the pull-up resistor according to the value of the corresponding inputs A_1 ,B_1) .

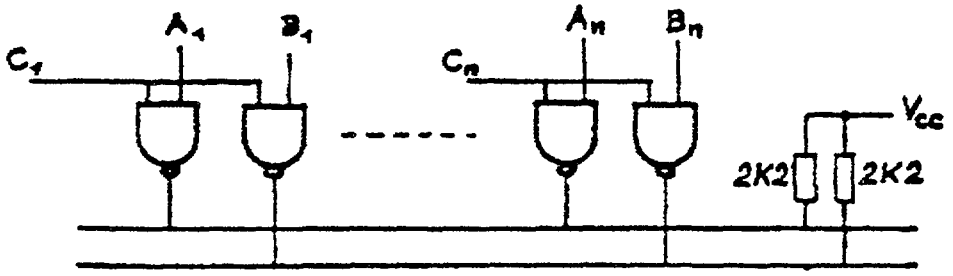


Fig. 3.2.4.: Bus with open collector gates.

Tri-state outputs. The output of a tri-state circuit can be in either of the two logic states, 0 or 1, behaving like a low-impedance sink or source, or it can be in a third, high impedance state. In this last case, whatever the logic state of the inputs, the output is effectively disconnected from the outside (in an open collector gate, the output is only disconnected when it is in logic state 1). The output is said to be enabled if it is not in the third state. A control input is required to enable/disable the circuit.

Let the 74LS125, or the corresponding CMOS type, represent the tri-state circuit. This IC is a quad non-inverting bus driver with separate enable inputs for each section. In Fig. 3.2.5, one of the sections is shown.

If enabled ($\overline{EN} = 0$), the LS125 circuit is able to sink or source a current of more than 20 mA as can be verified using R = 150 ohms. If disabled ($\overline{EN} = 1$), the circuit has a very high output impedance; this can be checked by using R = 100k, and by measuring the voltage at Y. It should be near V_{cc} or ground, depending on the switch position, irrespective of the voltage level at input A.

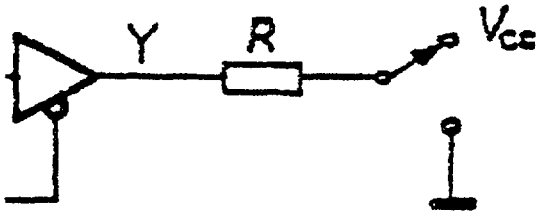


Fig. 3.2.5.: Output impedance of a tri-state circuit.

Tri-state circuits are specially useful in bus structures. You can make a simple circuit simulating a two-line bus, as illustrated in Fig. 3.2.6.

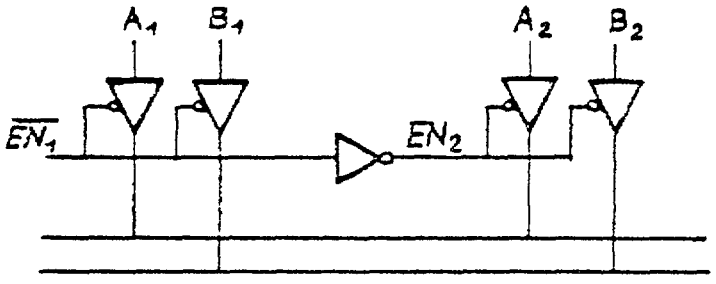


Fig. 3.2.6: Bus with tri-state gates.

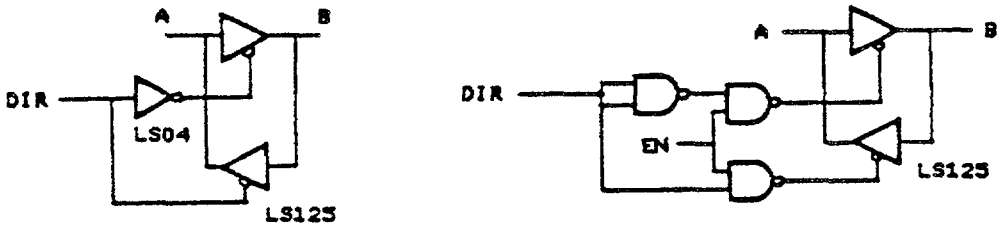
Note that the circuit design must assure that the different groups of gates will never be simultaneously enabled; otherwise the logic level of various lines will not be properly defined (some of the gates may be at 1 while others are at 0). This simultaneous enabling might even damage the circuits. (Compare this case with that of open collector gates.)

Transceivers. Transceivers are a useful class of circuits based on the tri-state principle. To clearly understand the functioning of a transceiver, assemble a circuit as shown in Fig. 3.2.7.

Observe that in the left circuit only one of the drivers is enabled. If DIR = 1, information flows from A to B, i.e. A acts as the input and B as the output. If DIR = 0, information flows from B to A: now B acts as input, and A as output. The circuit on the right behaves in a similar way but has the added feature of being able to tri-state A and B simultaneously, i.e. to isolate A and B from each other. The popular 74xx245 transceiver circuit behaves in this way.

Fig. 3.2.7:

Transceiver-type circuits



EXPERIMENT 3.3

DYNAMIC CHARACTERISTICS OF LOGIC GATES

OBJECTIVE

The objective of this experiment is to present the dynamic characteristics of logic gates, and to exploit these characteristics to implement rising and falling edge detectors.

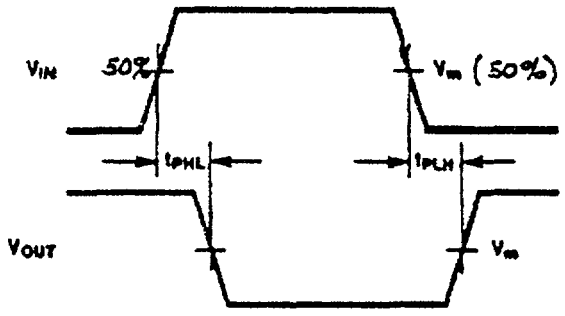
REVIEW

Propagation time is an important characteristic of a logic gate; it is defined as the time interval measured from the instant an input transition reaches 50% of its amplitude to the instant the corresponding output transition reaches 50% amplitude, as shown in Fig. 3.3.1.

Actually there are two propagation times shown in the figure, one for the rising and one for the falling transition. For a given circuit, t_{PHL} and t_{PLH} usually have similar values.

Fig. 3.3.1:

Propagation times



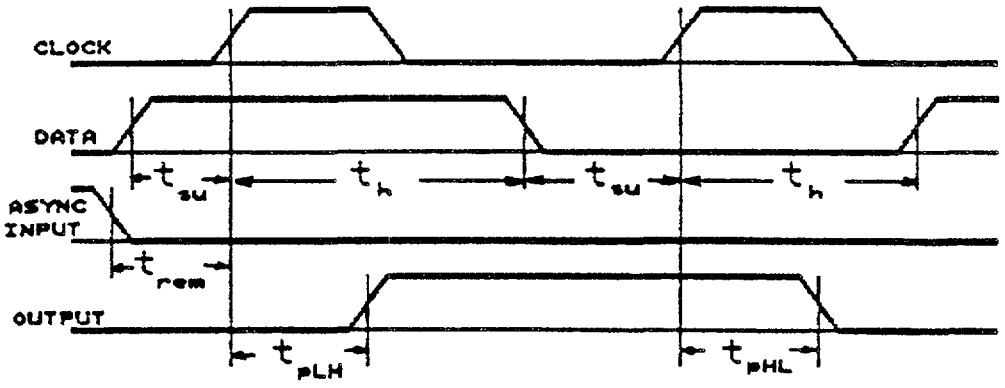
Propagation times for the different families and subfamilies vary within wide limits. The more modern circuits have significantly shorter times than the older ones. For example, the propagation time for a CMOS circuit of the HC series is about one order of magnitude shorter than that of the older CD series.

The propagation time must be measured with a specified load. This load should include a resistor to drain current from the output (avoiding, for example, the slow rise time above 3.5 V otherwise found in totem-pole outputs) and a capacitor to simulate the capacitance present in a real circuit (wiring and gate input capacitances).

For circuits other then simple gates, further time parameters must be specified. For edge triggered flip flops, for example, one defines pulse width, setup, hold and removal times in addition to the propagation delay time. The definitions are given in Fig. 3.3.2. The data sheets specify the relevant limits (either a maximum or a minimum) for each parameter. The removal time pertains to asynchronous inputs (for example, Preset and Clear), and the setup and hold times to the synchronous inputs (for example, J and K). The pulse width applies to all inputs. If the specified timing requirements are not fullfilled, eratic circuit behaviour is almost certain to result.

Fig. 3.3.2:

Dynamic characteristics in sequential circuits.



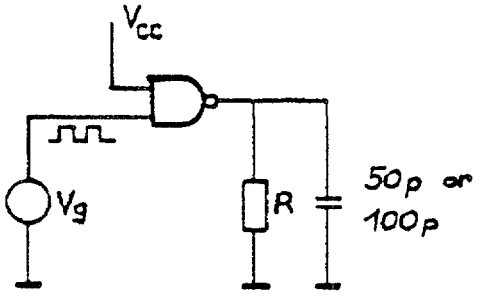
Propagation time

EXPERIMENT

The circuit of Fig. 3.3.3 may be used to measure the propagation time of a NAND gate. The generator should provide a square wave with fast rise and fall times. Compare the propagation times of circuits from different subfamilies, for example, TTL/LS, CMOS/CD, and CMOS/HD series. The rise and fall times of the gate output may be also determined. It is instructive to note that where V_{cc} can be varied in a large range (as for example, in the CD series), the propagation times decrease with increasing V_{cc}.

Fig. 3.3.3:

Setup for measuring propagation time.



Note that propagation time must be determined with a fast input signal. In practice, whenever slowly varying signals are encountered, the use of Schmitt trigger input gates is mandatory. At this point it is worthwhile to compare the rise times obtained with an LSOO and an LSI32 quad Schmitt input NAND gate, using a slowly varying input signal.

Edge detectors

Consider the circuits in Fig. 3.3.4. For the NOR circuit, the output gate will have one of its inputs at state I until A returns to state 0. After this, and for a duration equal to the propagation delay through one gate, both its inputs will be at 0. Thus Y becomes 1 for a short time at the falling edge of the input signal; the circuit acts as a falling edge detector. Similarly, the NAND gate circuit acts as a rising edge detector.

Any odd number of gates may be used to produce the necessary delay for operation of the edge detector. For example, an output signal three times wider than that in Fig. 3.3.4 is obtained with 3 delaying gates.

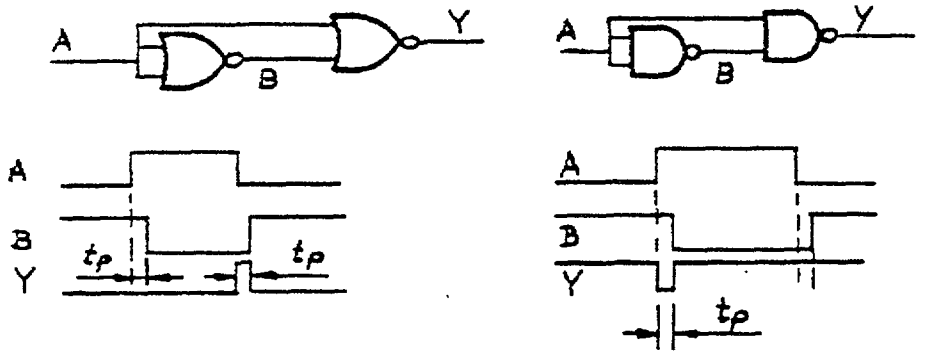


Fig. 3.3.4:

Edge detectors

The above edge detectors work well if the input pulses are rather sharp. Otherwise some delay should be added as shown in Fig. 3.3.5. The added delay obviously depends on the values of R and C.

Another interesting circuit is obtained by using an EXCLUSIVE-OR as the output gate in the edge detector circuit. You may draw a diagram of what is expected at the output in this case, and verify in the laboratory that the diagram is correct.

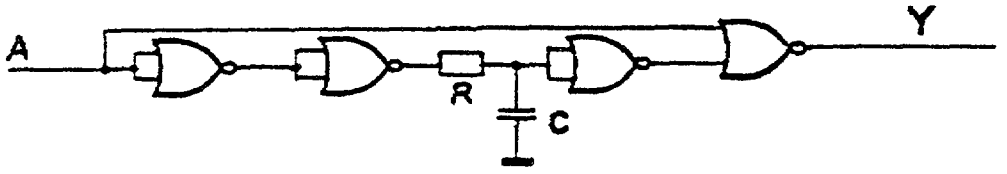


Fig. 3.3.5:

Edge detector for slower signals

Dynamic characteristics.

To determine the dynamic characteristics, one needs a set of time related signals. For example, the setup time of an LS74 D-type flip flop can be determined with the signals shown in Fig. 3.3.6, applied to the IC pins with the same name, and looking at the Q output. The Data signal is to be moved relative to the clock signal. While the setup time requirement is satisfied, the output will show a signal with approximately the same width as the clock. At some point, when the time between positive going edges of the Data and Clock signals is reduced, the flip flop will fail to operate.

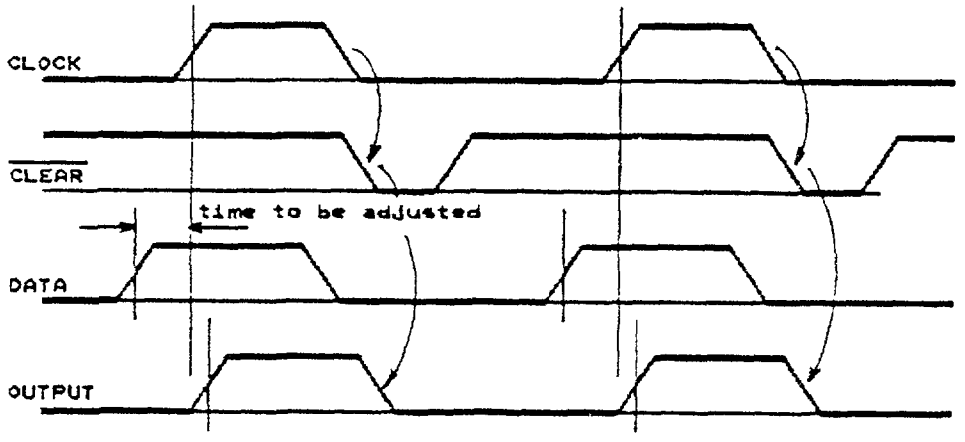


Fig. 3.3.6:

Signals used to determine setup time in a D type

flip flop.

Notes:

EXPERIMENT 3.4

COMBINATIONAL CIRCUITS

OBJECTIVE

To objective of this experiment is to practice with combinational circuits and to become acquainted with the main types of combinational integrated circuits available in the logic catalog.

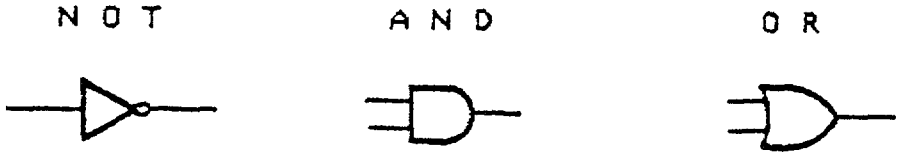
REVIEW

Digital circuits can, in principle, be implemented using only a pair of basic gates, either NOT and AND, or NOT and OR. Large or small numbers of gates, as necessary, may then be combined to execute whatever logical job the circuit is intended to perform. A small set of basic rules helps us to devise appropriate gate combinations once the job is clearly defined. A proper knowledge of these rules, or more exactly, theorems, is essential for the understanding of digital electronics. A review of these basic laws is given below with suggestions for their verification and application.

As in other fields, prefabricated blocks make life easier for the constructor. In fact, without them the design and assembly of complex circuits would be a long and tedious process. A knowledge of the available building blocks is, therefore, essential for anyone dealing with digital electronics. To help in this matter, a guided tour of the logic catalog, with some practical work along the way, is offered below. In this exercise we limit ourselves to combinational circuits; sequential circuits will be dealt with later.

The basic gates

The most elementary logic functions are NOT, AND and OR. Their truth tables are displayed in Fig. 3.4.1. Actually, only NOT and AND, or NOT and OR are required to generate any logic function. It is useful to write the truth tables in the form of Boolean equations:



A	Y
0	1
1	0

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 3.4.1: NOT, AND and OR truth tables

NOT : $Y = A$
AND : $Y = A \cdot B$
OR : $Y = A + B$

The bar indicates the complement operator; it is defined according to the NOT function truth table, that is, the complement of 0 is 1, that of 1 is 0: of couse,

$$\bar{A} = A$$

The dot indicates the AND operation (the dot, like in the expression for the usual product of two variables, is frequently omitted); again, the operation rules are defined by the AND truth table:

$$0 \cdot 0 = 0 \quad , \quad 0 \cdot 1 = 0 \quad , \quad 1 \cdot 0 = 0 \quad , \quad 1 \cdot 1 = 1$$

This can be written in a literal format:

$$A \cdot A = A \quad , \quad A \cdot \bar{A} = 0$$

The plus sign indicates the OR operation; again, the operation rules are defined by the OR truth table:

$$0 + 0 = 0 \quad , \quad 0 + 1 = 0 \quad , \quad 1 + 0 = 0 \quad , \quad 1 + 1 = 1$$

or, in literal form,

$$A + A = A \quad , \quad A + \bar{A} = 1$$

It is seen that both AND and OR operations are commutative,

$$A \cdot B = B \cdot A \quad , \quad A + B = B + A$$

The definitions of the AND and OR functions can be extended to more than two variables. For n variables, the AND function is defined as being 1 if, and only if, all the variables are I. The OR function is I if at least one of the variables is I. One may easily verify that the following laws hold:

Associative law: $(AB)C = A(BC) = ABC$, $(A+B)+C = A+(B+C) = A+B+C$
Commutative law: $AB = BA$; $ABC = BAC$, etc.
Distributive law: $A(B+C) = AB + AC$

Examples of these basic gates in the logic catalog are the series 74xxnn numbers 04 (hex NOT, usually called hex inverter), 08 (quad 2-input AND), 32 (quad 2-input OR), ll (triple 3-input AND).

The most versatile gates are the NAND and NOR, for they combine the AND and OR functions with the NOT function. Their truth tables and boolean expressions are shown in Fig. 3.4.2. Notice that the NOT function may be implemented with either a NAND or a NOR, with both inputs connected together.

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$Y = \overline{A.B}$

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overline{A+B}$

Fig. 3.4.2: NAND and NOR truth tables and boolean expressions.

Morgan's laws

One of the everyday tools of the digital circuit designer are the Morgan's theorems:

These laws are easily verified from the truth tables.

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

Variables A and B are arbitrary logic variables. In particular, we can substitute either A or B or both by their complements. We will then arrive at relations like the ones expressed graphically below:

The bubbled symbols are commonly found in circuit digrams when one wishes to stress the AND or the OR logical character of a function but the input variables are active low, e.i. their true value corresponds to logic state 0. For reference, a collection of Boolean algebra relationships is presented in Fig. 3.4.3.

As an application of Morgan's laws let us define a function by the truth table of Fig. 3.4.4. It is immediately clear that the function can be implemented by the circuit shown in the figure; this circuit requires one OR, one NAND and one AND gate - which, in practice, would mean three integrated packages. The corresponding Boolean equation helps us to do the same with a single package of NAND gates:

$$Y = (A + B).(A.B) = A.(A.B) + B.(A.B) = A.(A.B) \,.\, B.(A.B)$$

It is instructive to assemble this circuit and verify the truth table. The implemented function is known as an EXCLUSIVE-OR and is, actually, available in integrated circuit packages, for example, the 74xx86. The XOR may be used as a controlled inverter; you may try to design and verify the functioning of a 4-bit circuit whose outputs are either equal to or the complement of the inputs according to the value of a control variable.

Such an invertor is used in the internal circuitry of the LS135 EXCLUSIVE-OR/NOR gate; the option OR/NOR is selected by a control bit.

Fig.3.4.3 :

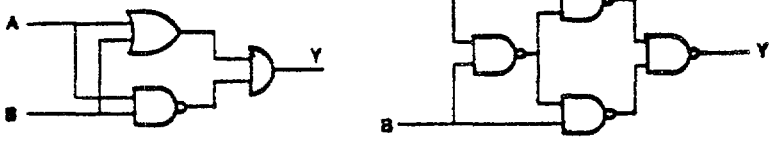
Some Boolean algebra relationships.

$$A + 0 = A$$
$$A \cdot 1 = A$$
$$A + B = B + A$$
$$A \cdot B = B \cdot A$$
$$A + (B \cdot C) = (A + B) \cdot (A + C)$$
$$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$$
$$A \cdot \bar{A} = 0$$
$$A + \bar{A} = 1$$
$$A + A = A$$
$$A \cdot A = A$$
$$A + 1 = 1$$
$$A \cdot 0 = 0$$
$$A + A \cdot B = A$$
$$A \cdot (A + B) = A$$
$$\bar{\bar{A}} = A$$
$$A + (\bar{A} + C) = 1$$
$$A \cdot (\bar{A}C) = 0$$
$$(A + B) + C = A + (B + C)$$
$$(AB)C = A(BC)$$
$$A + \bar{A}B = A + B$$
$$AC + \bar{A}B + BC = AC + \bar{A}B$$
$$(A + B)(\bar{A} + C) = AC + \bar{A}B$$
$$\overline{(AC + B\bar{C})} = \bar{A}C + \overline{B\bar{C}}$$
$$\overline{(A + C)(B + \bar{C})} = (\bar{A} + C)(\bar{B} + \bar{C})$$
$$\left.\begin{aligned}\overline{(A + B)} &= \bar{A} \cdot \bar{B} \\ \overline{AB} &= \bar{A} + \bar{B}\end{aligned}\right\}\text{De Morgan's theorems}$$

Fig. 3.4.4:

EXCLUSIVE-OR (XOR) truth table and circuits..

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



Another typical application of XOR gate is a parity generator. Try to design a 4-bit even parity generator, that is, a circuit with 4 inputs that gives a logic 1 at its output when an odd number of inputs are at logic state 1. You may verify your design before you test it, by looking at the logic diagram of the LS180 parity generator circuit.

Like the previous example, most of the more frequently used combinational circuits are available in integrated circuit form. We will now suggest a few experiments with representatives of the main types of these circuits, which are available in all logic families.

Multiplexers

EXPERIMENT

One function which is frequently required is to connect one of several lines to a given line. This function is analogous to that of a switch, or, if one wishes to do this simultaneously with more than one set of lines with a ganged switch, as represented in Fig. 3.4.5.

Taking a 2 line-to-1 line example, we want the following equation to be implemented

$$Y = A.S + B.S$$

where S is the variable that selects the inputs. The 74xxl57 circuit is a quad 2 line-to-l line multiplexer that implements the above function. More exactly, it implements the function

$$Y = E(A.S + B.S)$$

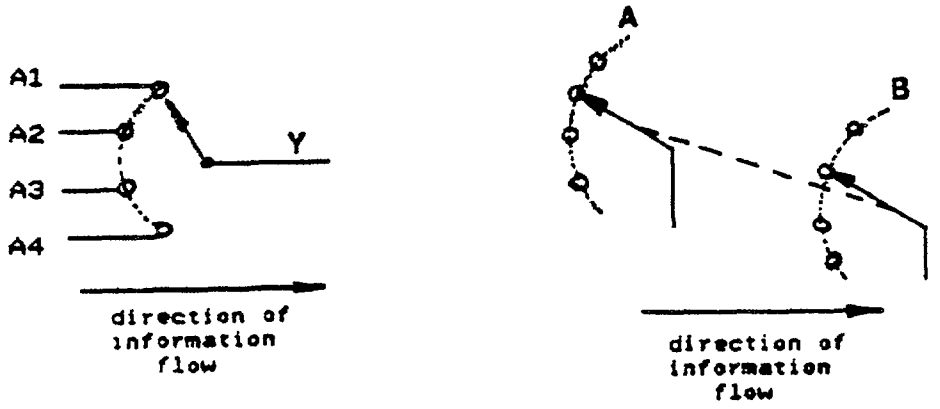


Fig. 3.4.5: Electro-mechanical multiplexers

The additional variable E enables the output to follow one of the inputs (selected by the S variable) if $\overline{E} = 0$; otherwise, Y = 0. We say "if $\overline{E} = 0$" because the variable actually applied to the circuit is $\overline{E}$, in the sense that a logic 0 applied at this input enables the circuit to perform its internal operation. It is usual to say that E is active low. The logic diagram of every one of the sections of the l57 is represented in Fig. 3.4.4. The 4 sections are simultaneously selected by the S variable. There are many applications for this multiplexer. For example, it is always better to do the switching of logic signals through multiplexers instead of mechanical switches, even when there is no need for dynamic switching (that is, when the setting of the switches is made outside normal circuit operation). This avoids the travelling of fast digital signals through long wires in their journey to the instrument panel and back.

As another example of multiplexer circuits, you may check the behaviour of the 8 line-to-1 line multiplexer 74xx151. Now, of course, 3 select lines are needed; and, as in the 157, an active low enable variable is available.

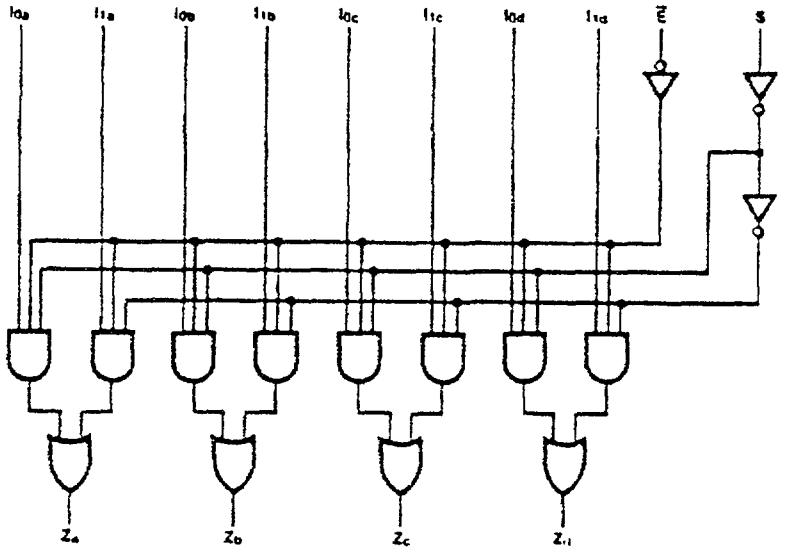


Fig. 3.4.6: Quad 2 line-to-1 line multiplexer (157).

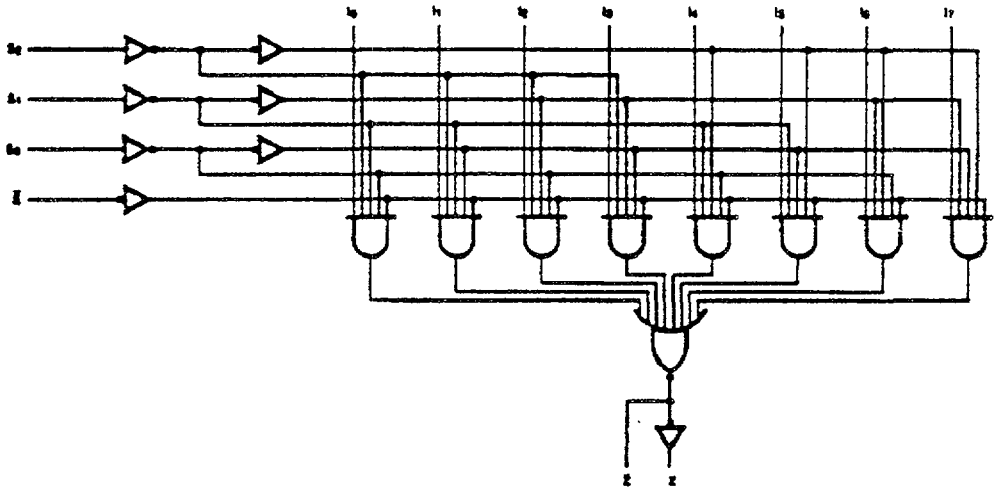
The implemented function is (I_i is the logic value of input data line i; the select variables are S_2, S_1, S_0):

$$Y = E\,(\,I_0\,\bar{S}_2\,\bar{S}_1\,\bar{S}_0 + I_1\,\bar{S}_2\,\bar{S}_1\,S_0 + \ldots\ldots + I_7\,S_2\,S_1\,S_0\,)$$

The 151 makes the complement of Y also available (output $\bar{Y}$). The logic diagram is shown in Fig. 3.4.7.

Fig. 3.4.7:

8 line-to-1 line multiplexer



An interesting application of multiplexers is to implement an arbitary logic function. For example, you should be able to implement the function f(A,B,C) defined in Fig. 3.4.8. You just connect A,B,C to the select lines and the input data lines to either ground or V_{cc} as appropriate. Actually, you may even use the 151 to implement a 4 variable function, f(A,B,C,D). Hint: associate A,B,C to the select lines; for each combination of these variables notice that Y is either 0 or I, D or $\bar{D}$.

Fig. 3.4.8:

Example of function to be implemented by a multiplexer

A	B	C	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

You may realize that used in this way the151 plays the role of an 8 x 1 or a 16 x 1 ROM (see Experiment 3.10).

Finally, let us note that the multiplexing function can be also implemented with open collector or tri-state gates suitably activated, so that a single gate is active at any one time. You may wish to try a design using one of the decoders presented below, to guarantee thsi simple activation.

Decoders/demultiplexers

A 1 line-to-n line demultiplexer feeds the signal from one line into another selected from a group of n lines; this is the function performed by a switch, or a ganged set of switches, in the manner shown in Fig. 3.4.5 but with the direction of information flow reversed. For example, a 1 line-to-4 line demultiplexer has 4 output lines Y_0 to Y_3; the boolean expressions for the various lines are:

$$Y_0 = D\,\bar{A}_1\,\bar{A}_0 \quad , \quad Y_1 = D\,\bar{A}_1\,A_0 \quad , \quad Y_2 = D\,A_1\,\bar{A}_0 \quad , \quad Y_3 = D\,A_1\,A_0$$

where D is the data line logic value and the A_i are the select variables. An important point to note is that the outputs are mutually exclusive, that is, only one line is selected at any one time.

The demultiplexer may also be looked at as a decoder. The A_i variables are then considered as labelling a set of addresses. With 2 variables, 4 different addresses may be specified (with n variables we may have 2^n specified addresses). The D variable then plays the role of an enabling variable. For each combination of the address variables 1 of 4 lines is activated. For a circuit obeying the above equations we would say that the line is activated high.

The two most popular decoders/demultiplexers are the 74xx139 (dual 1-of-4) and the 74xx138 (1-of-8). The logic circuit of one half of the 139 is shown in Fig. 3.4.9. If you translate the diagram to a Boolean expression you will obtain.

$$Y_0 = \overline{\bar{E}\,\bar{A}_1\,\bar{A}_0} \quad , \quad Y_1 = \overline{\bar{E}\,\bar{A}_1\,A_0} \quad , \quad Y_2 = \overline{\bar{E}\,A_1\,\bar{A}_0} \quad , \quad Y_3 = \overline{\bar{E}\,A_1\,A_0}$$

The outputs are active low (at most one output is in state 0, all the others being in state 1). If the circuit is looked at as a decoder (as is the case in most applications), then E is an active low, enabling variable (all outputs will be high if $\bar{E} = 1$). If the circuit is used as a demultiplexer then $\bar{E}$ is the data input line.

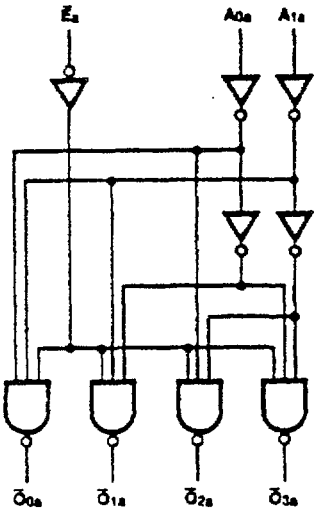


Fig. 3.4.9: 1-of-4 decoder/ multiplexer (139).

You may also verify the truth table of the 138, a circuit used in very many applications. Its logic diagram is shown in Fig. 3.4.10. As you see from the diagram, the equations for the outputs are analogous to those of the 139; but instead of a single enabling variable, we now have three connected to one AND gate; two are active low, one active high. The circuit thus contains a more flexible enabling control, useful in many applications.

The 138 is a standard circuit in memory and input/output port address decoding in microprocessor circuits. In this application, 3 address lines are connected to the select inputs; frequently, one or more of the enabling inputs are also connected to address lines. The output mutually exclusive lines are then connected to the chip select (enabling) inputs of the memory or port circuits. (We have refered to mutually exclusive outputs more than once. You may wish to design a circuit to experimentally determine whether this is true or not.)

The 138 is also a very appropriate circuit for the control of open-collector or tri-state based multiplexers. You just need a bit of skill and patience to verify this yourself by

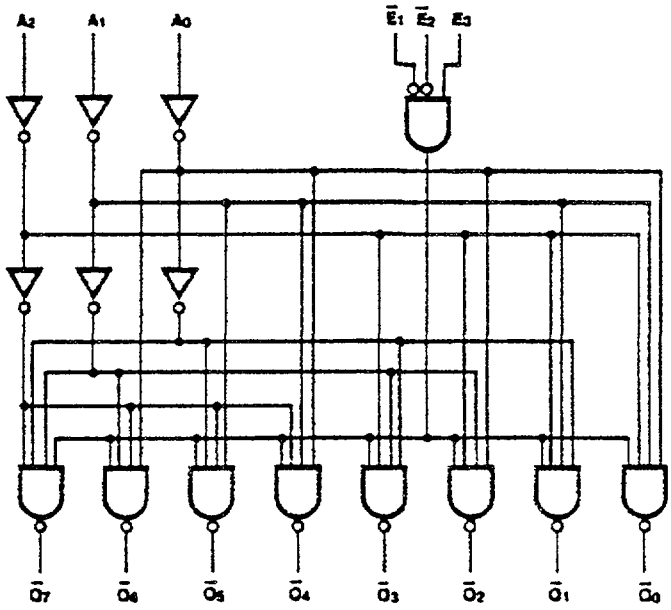


Fig. 3.4.10:

1-of-8 Decoder/ demultiplexer (138)

designing, for example, a system that multiplexes 6 sets of 4 outputs each onto a 4 line bus (the 74xx240 is a suitable tri-state circuit to this purpose). Such a system may be used in the display section of a scaler.

Like the multiplexer circuits, decoders may also be used to implement abritrary functions. Recall that any logical function can be expressed as a sum-of-products. Products in which all the function variables (complemented or not) appear once, are called minterms; an logical function can be expressed as a sum of minterms. For example, a given function f(A,B,C) may be expressed as

$$f(A,B,C) = \overline{A}\,B\,C + A\,\overline{B}\,C + A\,B\,\overline{C}$$

Notice that each output of a decorder corresponds to a minterm of a function of the select variables. Thus you may, for example, easily implement an arbitrary function of 3 variables by using a 138 decoder and appropriate OR gates.

Digital comparators

A digital comparator is a combinational circuit that compares 2 numbers of n bits, A and B. The three possible results of the comparison are A < B, A = B and A > B. If one is only interested to check whether A = B or A ≠ B, then ANDing the outputs of EXCLUSIVE-NOR (XNOR) gates is enough to produce the active high A = B signal:

$$(A = B) = \overline{(A \oplus B) \ldots (A \oplus B)}$$

Frequently, one is interested in circuits that are able to distinguish the three possible results. Such a circuit for 1 bit numbers is presented in Fig. 3.4.11, where the truth tables and corresponding equations are also shown.

Two very popular comparators are the 4 bit magnitude comparator 74xx85 and the 8 bit equality detector 74xx688. The 85, in addition to the A and B inputs, has inputs that allow the circuit to be cascaded. Thus, the 85 may be used to compare numbers with an arbitary number of bits: the outputs A < B, A = B and A > B of one stage are then to be connected to the corresponding inputs of the next higher (more significant) stage.

Fig. 3.4.11:

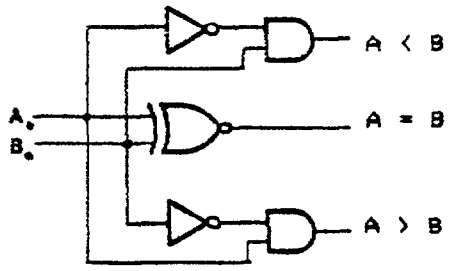
1-bit magnitude comparator

A_0	B_0	A < B	A = B	A > B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

$$(A>B) = \overline{A_0} \cdot B_0$$

$$(A=B) = \overline{A_0 \oplus B_0}$$

$$(A>B) = A_0 \cdot B_0$$



One of the frequent applications of these circuits is to select memory chips (that is, to enable write or read operations). After experimenting with the 85, you may wish to design and verify an address decoder that is able to map an 8k memory into a space beginning at any 8k boundary of a 64k memory space (that is, at 0000H, 2000H, etc.) The beginning address is to be chosen by suitable placement of jumpers that force some of the inputs of the 85 to become either 0 or 1.

The 688 also finds an interesting application as a word recognizer in the trigger circuitry of logic analyzers. A trigger signal is generated whenever the input word (applied, say, to the P inputs) matches a preset word (applied to the Q inputs).

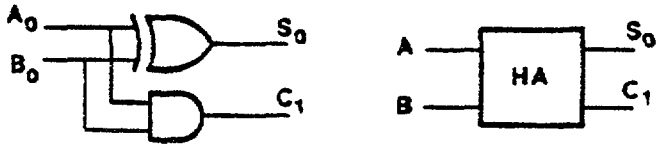
Adders

An adder is a circuit designed to perform the additon of two numbers. Consider the addition of 1-bit numbers, A and B ; the truth tables for the sum bit S and the carry bit C are shown in Fig. 3.4.12, together with the circuit that implements the operation.

Fig. 3.4.12:

Sum of 1-bit numbers

A_0	B_0	S_0	C_1
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

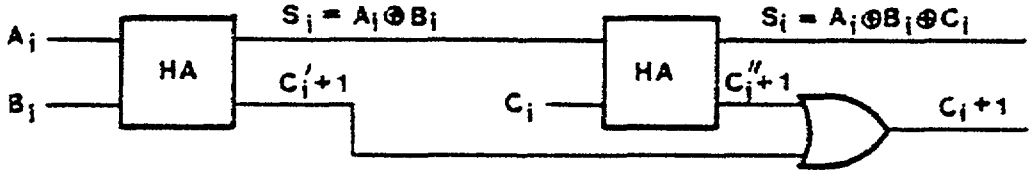


The circuit is also given a compact representation, where the letters HA stand for Half Adder. This name is related to the following algorithm for summing n-bit numbers: first sum the least significant bit to obtain S_0 and C_1 ; next obtain each sum bit S_i (first sum A_i and B_i, then sum C_i to this partial result) and carry C_{i+1} (by taking into account the carries of both sums performed to obtain S_i). This algorithm is clearly expressed in symbols in Fig. 3.4.13. The circuit to obtain S_i and C_{i+1} is called a full adder.

The 74xx283 is an example of a binary full adder. In addition to the inputs for the A and B bits, it has a carry input that allows the circuit to be easily cascaded to obtain the sum of numbers of an arbitrary number of bits.

Fig. 3.4.13:

Full adder



A TTL adder can do an addition in a few nanoseconds. As arithmetic units, they are used whenever the comparatively slow speed of a microprocessor cannot be accepted. A typical example in nuclear electronics is in the sliding scale correction of successive approximation ADCs (see TECDOC-363).

Priority encoders

A priority encoder is an n-input circuit which outputs a code giving the address of the highest numbered line that is activated. Consider a 4-input circuit and number the lines from 0 to 3; the priority encoder would give a 2-bit output word, A_1A_0 indicating in binary code the highest line that is activated. You may verify that to satisfy this requirement the encoder should implement the following equations:

$$A_1 = I_2 + I_3 \quad , \quad A_0 = I_3 + I_1 \bar{I}_2$$

Note that I_0 does not appear in these expressions. In practice we would probably wish to have an output G showing that at least one line is activated; and it would be nice to add an enabling input E, as shown in Fig. 3.4.14, on the following page.

If you add these features you will end up with a circuit analogous to the 8-line to 3-line priority encoder 74xx148. It is instructive to verify the behaviour of the 148, especially the feature of it being sensitive only to the highest-numbered line activated. Priority encoders find an obvious application in A/D flash type converters, but their main application is in microprocessor circuits.

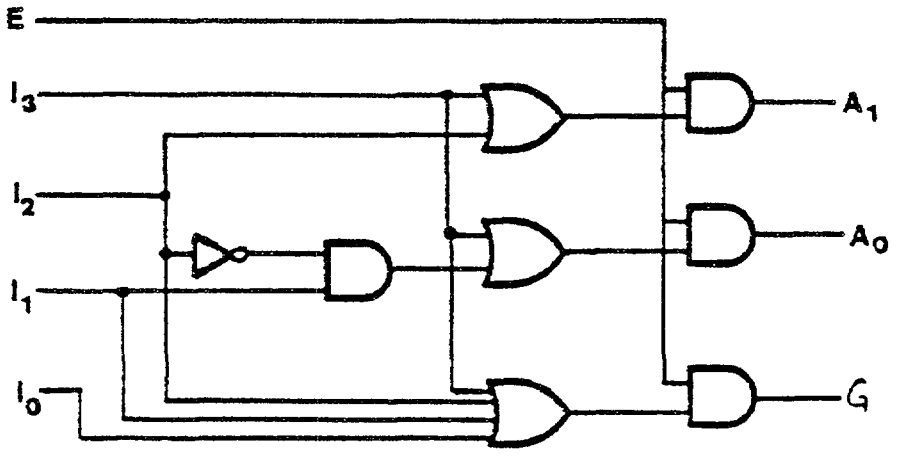


Fig. 3.4.14:

4-line to 2-line priority encoder

Code converters

Several codes are used in digital systems. The "natural" code is the binary code, where numbers are represented according to the base 2 numerical system, with HIGH standing for 1, and LOW for 0. Binary is not, however, a compact code: it requires more digits than other codes (for example, the decimal code) to represent a large number. We will just refer to a few widely used codes.

In the hexadecimal code bits are grouped in sets of 4 (starting from the least significant); the group is represented by the symbols 0 to 9, A to F according to its binary value. All 16 combinations of the 4 bits are allowed. To translate, by hand, one of these codes into the other is immediate; in this sense, the hexadecimal code is just a short-hand notation. The hexadecimal code should not be confused with the 1-out-of-16 code, which associates the state of 1 of 16 lines to each value of a 4 bit group.

The BCD (binary-coded decimal) code is also based on 4-bit groups. Each group, however, may only take 10 values, from 0 to 9. This makes life more complicated as far as translation from, or into, binary is concerned. But it is an enormous simplification when one wishes to show some result in a decimal code. The BCD code (and the decimal code) should not be confused with the 1-out-of-10 code.

The last code we wish to reference is just used for display purposes. It is the familiar 7-segment display code. The 7 bits of this code are each associated with an LED in the form of a segment; and, to allow reading in the form of arabic numerals, the segments are placed as shown in Fig. 3.4.15. (The decimal point frequently seen in these displays is also shown.)

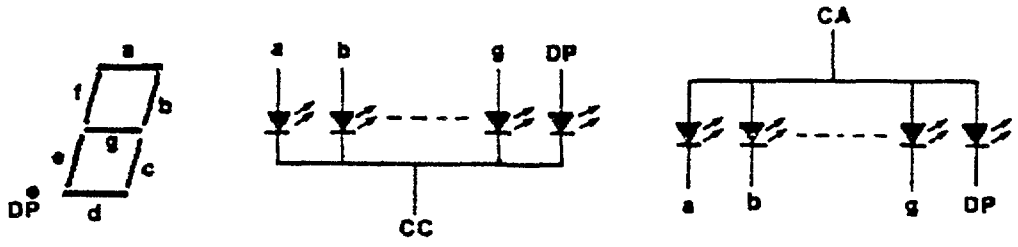


Fig. 3.4.15: 7-segment digit and circuits for the CC (common cathode) and CA (common anode) varieties.

Code converters are circuits that convert from one code into another. An example is the 74xx154 that converts a 4-bit binary code into a 1-out-of-16 code. We may also look at this circuit as a 4-line to-16-line decoder.

A most important converter in nuclear electronics is the BCD to 1-out-of-10 code converter. The 74xx42 is an example of the available integrated circuits. Again, the circuit may be looked at as a decoder. Later on you may wish to use a 42 associated with counters (usually synchronous counters; asynchronous ones produce glitches as discussed in Experiment 3.8).

The 74xx47 is a BCD to 7-segment converter. It converts from the 4 bits of the BCD code into the 7 bits necessary to drive a 7 segment display. In scalers made with decade counters (discussed in a later exercise) one generally uses a single BCD to 7-segment converter for the whole set of decades. This, of course, implies that different slots of time are to be allocated to the conversion of each decade; and that the various decades are multiplexed to the converter. An 74xx138 may then be used to control the system operation, as suggested earlier. (You may try to design such a system if you already know the sequential logic involved in the process.)

Programmable circuits

In our tour of the logic catalog we included representatives of the main functions available in integrated circuits; if you browse over the data books you will find some more, generally implementing more specialized functions.

A special reference must be made to an altogether different class of circuits: programmable circuits. They are being used at an ever increasing rate. Below we refer specifically to the so-called PAL (Programmable Array of Logic) circuits.

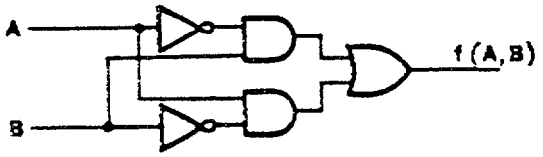
First we recall that any Boolean function can be expressed as a sum of products. The products contain any number of the function variables, complemented or not. The sum contains less than 2^n products for a function of n variables. For example, we may have for a function of two variables, f(A,B).

$$f(A,B) = \overline{A}B + A\overline{B}$$

This function may be obtained with the circuit shown in Fig. 3.4.16.

Fig. 3.4.16:

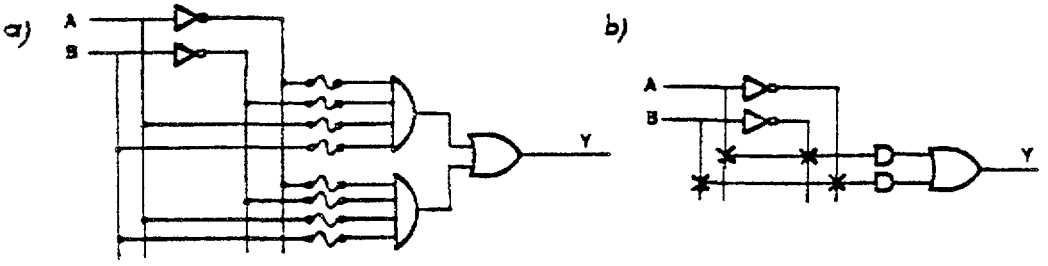
Circuit for f (A,B) = AB + AB



We may, however, wish to design a circuit in which any arbitrary function of two variables could be implemented. Such a circuit is shown in Fig. 3.4.17a. The fuses are to be blown whenever the corresponding variable (or complemented variable) does not appear in the function expression; if an AND gate is not used, then we leave all inputs connected (its output will then be LOW because variables are ANDed with their complements). A simple way of presenting the schematics of Fig. 3.4.17a is shown in Fig. 3.4.17b, where the connections corresponding to the previous examples, are shown by crosses (when no cross is present, there is no connection).

Fig. 3.4.17:

Implementing an arbitrary function fo two variables.



In the circuit of Fig. 3.4.17 you see that we have a OR gate with predetermined inputs (the outputs of all AND gates), and a programmable array of AND gates (we may program, i.e. connect or not any input variable or its complement to any AND gate). This type of circuit is referred to as a PAL.

As an example of the available integrated PAL circuits, we show in Fig. 3.4.18 the logic diagram of the PAL16L8, a 20-pin package PAL.

It can be seen that the 16L8 may accept as many as 16 input variables and produce as many as 8 output variables, but limited to an input-plus-output total of 18 variables. Notice that all outputs are tri-state, with the enabling variable being determined by an arbitrary product of the input variables. Notice also that 6 of the possible sum-of-products outputs are inputed back to the AND array; this allows for expansion of the maximum number of terms that can be used in an expression (you see from the diagram that a single sum is limited to a maximum of 7 terms).

The PAL allows the implementation, in a single package, of logic that may otherwise require quite a number of packages if implemented using the standard fixed functions commercially available. For this reason, the use of PALs is increasing in newly designed equipment.

To design with PALs one needs a PAL programmer and appropriate software to drive it. Given the tools, it is an easy job. From the maintenance point of view, they pose a problem. To program a new PAL, one needs to know the equations that are to be implemented, and this information is, to say the least, very difficult to obtain.

Finally, let us note that there are many types of PALs available, including types with sequential logic (registers). There are also other types of programmable logic. For example, there are circuits in which the AND array is fixed, and the OR array is programmable, and circuits in which both arrays are programmable. In a later experiment, ROMs are referred to, and these are also programmable circuits in which logical functions may be implemented.

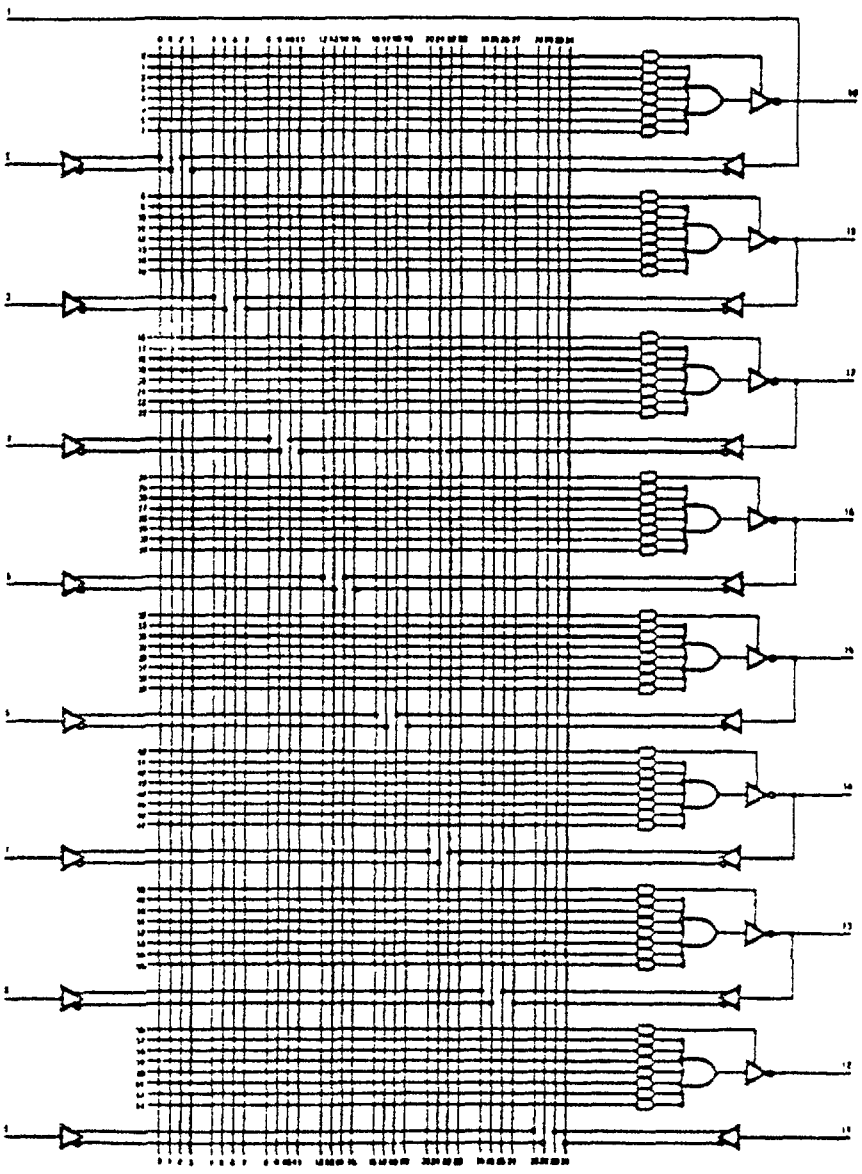


Fig. 3.4.18:

Logic diagram of PAL 16L8

Notes:

EXPERIMENT 3.5

SOFTWARE TOOLS FOR PROGRAMMABLE LOGIC

OBJECTIVE

The objective of this experiment is to introduce the software tools required for programming PALs.

REVIEW

Programmable arrays of logic (PAL circuits) are easily programmed with available software tools. To be specific, we refer to CUPL, a well known program that runs on any IBM personal computer.

The input to the program is a logic description file that describes the boolean equations to be implemented and assigns pins to all input and output variables. The main output of the program is a JEDEC file to be sent to a PAL programmer, the piece of hardware that actually burns the appropriate PAL fuses. The program may also output a documentation file, an error list file and a file to be used for computer simulation of the programmed device.

The languge used in the logic description file has the following elements:

- variables and indexed variables (these allow list notation, for example, [A7..A0] meaning the set of the 8 individual Ai variables). The variable name may have an extension (for example, .CK, .D, .OE);
- reserved words and symbols (for example, PIN and $);
- numbers (binary, octal,decimal and hexadecimal bases may be used);
- comments (to help readability of the description).

The language syntax allows the use of the following elements:

- logic operators: NOT (!), AND (&), OR (#) and XOR ($), here listed in order of decreasing precedence, and the operators related to the advanced operations referred to below;
- expressions: for example, (A&B#!A&!B)
- logic equations:used to assign one variable, or its complement, to the value of an expression. To increase readability of the programmed equations, intermediate variables may be defined. Thus, instead of Y = A&B#C&D one may write Y = X1#X2 if X1 and X2 are defined as X1 = A&B, X2 = C&D.

The program recognizes a number of statements. The most basic one associates a pin number to a variable;it uses the general format: pin number = [!]variable[.ext]. Another frequently used statement is FIELD. It takes the general form: FIELD name = [variable..variable]; a specific example is FIELD A = [A7..A0].

A number of advanced operations are also possible. These include so called Set operations, Equality operations, and Range operations. They are described in detail in the CUPL program manual.

As in the case of most other computer programs, it will be helpful to look into the program manual whenever difficulties arise, or when the available options are to be selected.

Programming a PAL16L8.

EXPERIMENT

To practice with the program, and to understand some of the tricks involved, first write and run a file to implement the basic functions AND, OR, NAND, NOR, XOR and XNOR in a PAL16L8. As may be seen in fig.3.4.18, the output signals of this device are the complements of the sum-of-products performed in the inner circuitry. You should see the consequences of this fact if you look at the expanded equations in the documentation file.

Next, graduate to a larger problem and design, for example, a 4-bit asynchronous adder. Among other things, you will appreciate the advantages of being able to use some of the PAL outputs as input variables in other products.

Use any word processor (able to work in standard ASCII mode) to prepare your logic description file. The template that comes with the program will help you in writing a clear, well presented description file.

Registered PALs, that is PALs with flip flops included in their circuitry, are programmed in a similar way. The logic equations are writen for the D inputs of the various flip flops, which are updated by a common clock signal. You may see a specific example in the logic implemented in a PAL 20R8 type of device for the MCA computer link, described in the special project "ADC computer link".

EXPERIMENT 3.6

TIMING CIRCUITS AND OSCILLATORS

OBJECTIVE

The objective of this experiment is to introduce monostable and other timing circuits, along with some of their applications.

REVIEW

Timing circuits, in the form of monostables and astables or oscillators, are essentially analog circuits that have widespread uses. Monostables are frequently made out of gates, specially if there are some unused gates left over in a package. Integrated monostables with good precision specifications are available in all the logic families. The designer only needs to add the CR timing elements to have a working circuit. The old 555 timer is still very much used either as a monostable or as an astable. It is worthwhile to become familiar with it. For clock applications, quartz controlled oscillators are a natural choice because they give the best precision and can be easily implemented using integrated inverters.

Monostables build with NAND and NOR gates

EXPERIMENT

Simple, low precision monostable circuits can be made using NOR and NAND gates in circuits as shown in Fig. 3.6.1.

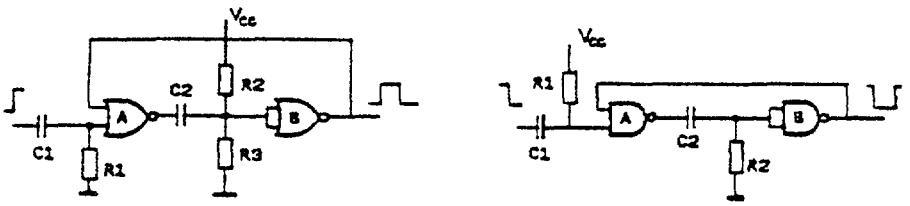


Fig. 3.6.1: Monostable circuits

Let us refer first to the NOR gate circuit. In the quiescent state, the output of gate B is at 0; therefore both inputs of gate A are at 0. The circuit is triggered by a low-to-high transition. The input signal is differentiated by C1-R1, typically with a short time constant. (Determine reasonable values for a time constant of 50 ns.) The output of gate A goes LOW; this signal is passed through C2 to the input of gate B. The output of this gate goes HIGH, thus causing gate A output to stay LOW even if the differentiated input signal has returned to zero. Capacitor C2 charges up with a time constant C2xR2||R3 (the sign || means the parallel of the two resistors) until it reaches about 1.5 V (for LS

gates). At this value, gate B switches back to its quiescent state. The output pulse duration is about 0.7xC2xR2||R3. It is instructive to assemble the circuit and observe the waveforms at various circuit points. Choose values for C2, R2 and R3 to obtain a monostable width of about 1 microsecond. The resistor values should be compatible with the driving requirements of the gate used. It should be clear that the CMOS gates allow larger resistors to be used. Note that resistor R3 is needed in TTL circuits because the pulse amplitude at gate A output is limited to about 3.5V; this would not be enought to pull the voltage at gate B input below 1.5V if its quiescent value were 5V. For CMOS gates, R3 may be deleted.

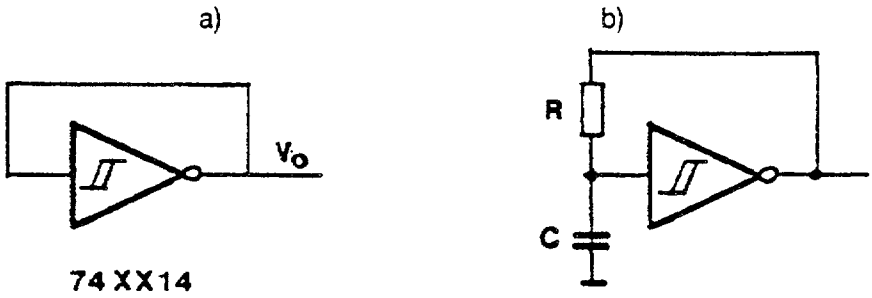
The functioning of the NAND gate monostable can be described in a similar way. Choose values for the components to obtain the same monostable width as in the previous circuit. Notice that while the NOR monostable is triggered by a positive edge, the NAND circuit is triggered by a negative edge. Verify the following; that if the differentiating network C1-R1 is taken out of the circuit, and a rectangular pulse is applied to the input, the output width is still determined by the time constant of the circuit (and not by the width of the input signal).

Astables built with inverters

Astable circuits can be easily built with NAND, NOR, or with simple inverter gates. A Schmitt trigger inverter oscillator is shown in Fig. 3.6.2a. It oscillates at a high frequncy, determined by the propagation time of the inverter. It can be slowed down, as indicated in Fig. 3.6.2b. In this case, the frequency is essentially determined by the values of R and C; it may be noted that the voltage across C varies between about 0.8V and 1.6V. (Discuss the reason why the duty cycle is not 50%.) Observe what happens if a normal (non-Schmitt) inverter is used in the diagram of Fig. 3.6.2a. Of course, any odd number of gates may be used in series in circuits similar to those of Fig. 3.6.2.

Fig. 3.6.2:

Simple oscillators



Integrated circuit timing circuits

The 555 is a very popular timing IC that can be used with any supply voltage in the range of +5 to +15V. A simplified block diagram of the internal connections is shown in Fig. 3.6.3. The outputs of the two comparators are connected to an RS flip-flop; the negative input of the R comparator is at 2/3 V_{cc} and the positive input of the S comparator is at 1/3 V_{cc}. The Q output of the flip-flop drives the base of a transistor. Let us consider the operation of the circuit as a monostable. External connections are made in this case as indicated in Fig. 3.6.3.

In the stationary state, the output Q of the flip-flop is at logic 1, and the transistor is saturated. The output of R comparator is LOW (R=0), and the S comparator is also LOW (S=0). When a negative trigger signal with enough amplitude to pull the negative input of the S comparator below 1/3 V_{cc} appears, the flip-flop is set (Q=1), and the discharge transistor is cut off. The capacitor starts charging through resistor R. When its voltage reaches 2/3 V_{cc}, the flip-flop is reset by the action of comparator R, causing

the discharge transistor to conduct again. The output pulse, taken from the Q output of the flip-flop, has a width T determined by the charging time of the capacitor from 0 V to 2/3 V_{cc}. Show that $T = 1.1xRC$. (Note: not all connections that should be made in practice, are shown in Fig. 3.6.3. For details refer to the data sheet of the 555.)

We may use Fig. 3.6.3 also to refer to retriggerable monostables. Suppose that you add to the circuit a transistor in parallel with C. If the transistor is cut off, operation is as described above. However, if the transistor is set to saturation before the comparator R resets the flip-flop, it quickly discharges C, and the charging of C starts again from the beginning. If the transistor is set to saturation for every trigger pulse, the circuit is called a retriggerable monostable. The Q output stays HIGH until the flip-flop is eventually reseted.

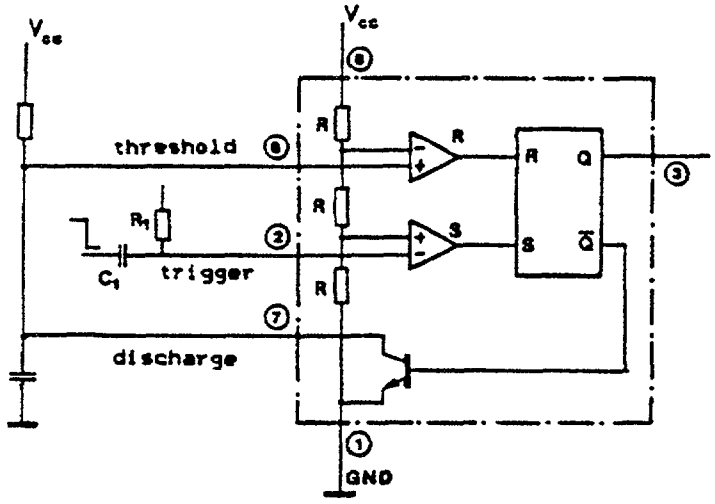


Fig. 3.6.3:

Block diagram of the 555, and connections for monostable operation.

The 555 is also very useful as an astable circuit. Its duty cycle can be varied within wide limits. Connections relevant to the timing operation are made according to the diagram of Fig. 3.6.4. Refer to the 555 data sheet to complete the circuit. Notice that in this circuit, the capacitor is discharged through R_B and charged through R_A.

The operation of the circuit can be described as follows: if the input Q is LOW, then $\overline{Q}$ is HIGH, and the discharge transistor is saturated. The voltage at the comparator inputs is decreasing. When it reaches 1/3 V_{cc} comparator S sets the flip-flop, thereby cutting off the discharge transistor. The capacitor starts charging up until its voltage reaches 2/3 V_{cc}. At this value the comparator R resets the flip-flop, and the whole process is repeated again. For the circuits to operate, it is necessary that the terminal 2 is allowed to go down below 1/3 V_{cc}; therefore, we must use $R_B < 2R_A$. Show and verify that, in one cycle, $Q = 1$ during a time interval $T_A = 0.7xR_A C$, and $Q = 0$ during $T_B = 0.7xR_BC$.

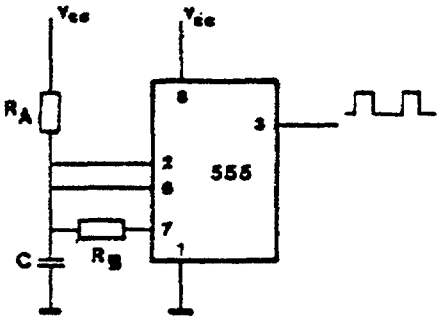


Fig. 3.6.4:

Astable operation of 555

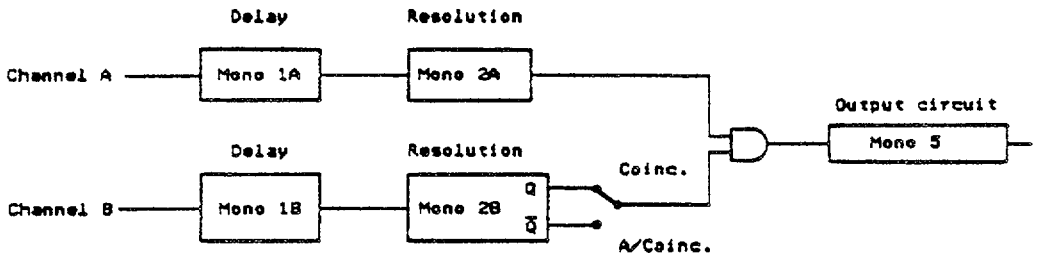
As stated above, the duty cycle of this astable may be adjusted within wide limits; in particular it may be set to 50%. There are applications (for example, in high voltage power supplies) where this 50% value is critical; in these cases, use of a flip-flop to obtain an exact square wave is recommended.

A 74xx series monostable

Several monostable circuits were specially designed for use with the 74xx series. Examples are the 74221 and the 74HC221. These are dual monostables with reset. Each monostable may be triggered either with a rising edge (B input, Schmitt trigger type), or by a falling edge (A input). The width of the pulse is again defined by external components R and C. It is $T = 0.7RC$. You may use these circuits to build a simple coincidence/anticoincidence unit following the block diagram of Fig. 3.6.5.

Fig. 3.6.5:

Block diagram of coincidence/ anticoicidence



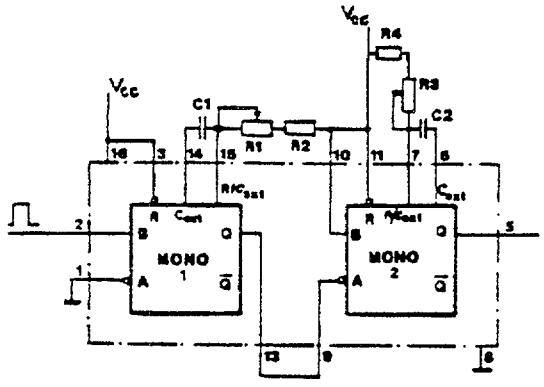
Using the TTL circuit, the width of the monostable can be varied from 50 ns upwards. Let us design the unit to have a variable delay from about 0.2 to 2 microseconds in each channel, and a resolution variable from about 0.1 to 1 microsecond. This implies that the resolution monostables are adjustable from roughly 50 to 500 ns. Assuming that the input signals are NIM positive logic signals, the rising edge trigger input is used in both delay monostables. The Q output of the delay monostables is connected to the falling edge trigger input of the resolution monostables. The connections for the monostables of Channel A are shown in Fig. 3.6.6. The minimum and maximum values of the delay are C1xR1 and C1(R1 + R2). With C1 = 100pF, R1 = 2.7k and R2 = 25k, we should be close to the desired values for the delay. You should find the appropriate values for monostable 2, and assemble the circuit for testing purposes.

The coincidence detector may be a simple AND or NAND gate. A single 74LS00 package is enough to implement the coincidence detector and an output monostable to produce defined output pulses (say, of 200ns width). Design and test the complete unit. Show that the unit makes coincidences or anticoincidences according to whether Q or Q of one of the resolution monostables is the input to the detector gate.

The 74xx series also has monostables of the rettrigerable type, for example, the 123. These type of monostables are sometimes referred to as missing pulse detectors because of their ability to detect a missing pulse in an otherwise regular pulse train. You may wish to show how connections are to be made for this application (using the 123 or the 555 with an external transistor).

Fig. 3.6.6:

Delay and resolution monostable connections.



Crystal oscillators

Whenever one wishes to have good frequency stability, the use of crystal oscillators is recommended. There are many ways in which these oscillators can be implemented. Two of them are shown in Fig. 3.6.7.

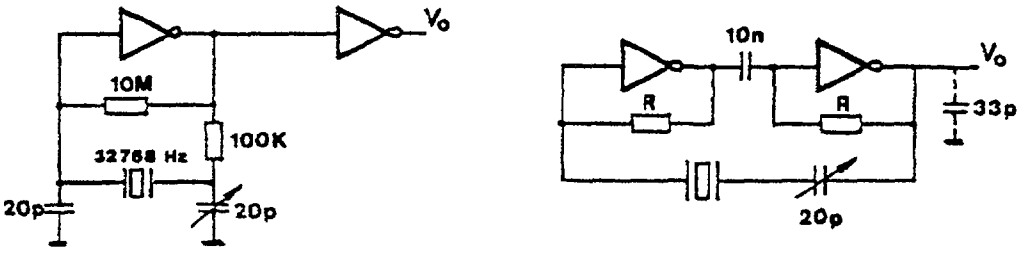


Fig. 3.6.7: Crystal oscillator circuits

In the circuit on the left, a single CMOS-type inverter is used in the oscillator. A suitable IC is, for example, the 74HC04. The crystal frequency is such that division by 2E15 yields one second time marks. The variable capacitor allows tunning to the exact frequency. There are integrated ripple counters designed specially to accomplish this division.

The circuit on the right can be used up to 100 MHz, depending on the speed of the inverters. The two inverters of the oscillator loop are biased into their linear region of operation, where the voltage gain is around 5V for TTL circuits. The crystal operates near the series resonance and the frequency may be tuned by adjusting the value of the capacitor in series with the crystal. The value of the resistors is to be chosen according to the inverter family used; for example, 1M for CMOS, 1K for TTL. The 33 pF capacitor may be necessary to suppress undesired high frequency oscillations. Test this circuit using a 10 MHz crystal and the 74LS04 inverters.

Notes:

EXPERIMENT 3.7

LATCHES AND FLIP-FLOPS

OBJECTIVE

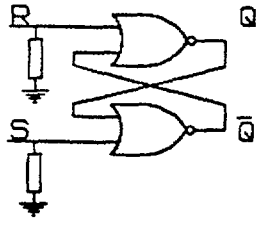
The objective of this experiment is to present the main functional and timing properties of latches and flip-flops, and to get acquainted with the various device types available in the logic catalog.

REVIEW

Latches and flip-flops are the basic memory building blocks of sequential systems. They both have similar operation command inputs, one update command input, and a pair of complementary outputs. They differ from each other in an essential way. Latches are transparent, that is, their output follows whatever is commanded by their inputs while the updatepulse lasts. The output of flip-flops changes only, at a well defined time (independently of the duration of the command pulse). There are various types of latches and flip-flops. They will be described by the functions they perform and, for flip-flops, attention will be called to a particular timing property. This property is the time at which the command inputs are sampled, that is, the time at which the values present at the input are relevant to the operation of the flip-flop. A number of experiments related to these basic properties is suggested. Special applications, like counters and shift registers, are dealt with in a later experiment.

The RS latch

An RS latch is a bistable circuit. It can be made of two cross-connected NOR gates as shown in Fig. 3.7.1. With no signals applied to the R and S inputs (R=S=0), the latch will stay in one of its two possible states, either Q=0 or Q=1, due to the feedback introduced by the cross-connection.



S	R	Q
0	0	0 or 1
0	1	0
1	0	1
1	1	forbidden

Fig. 3.7.1: RS latch: circuit and state table.

If the R input is forced in the HIGH state, Q becomes LOW and stays there even after R returns to LOW. Actually, as may be seen from the diagram, for this condition to be obtained it is only required that R stays HIGH for a time equal to the propagation delay through the two gates. Similarly, if S is momentarily forced HIGH, Q becomes HIGH and will stay there after S returns to LOW. Thus we have a way of setting (Q=1) or resetting (Q=0) the latch; while S=R=0 the latch will not change its state. This is summarized in the state table of Fig. 3.7.1. Clearly, if the latch is in state Q=1, forcing S to the HIGH state has no effect; and similarly for the R input when Q=0. If S and R are simultaneously HIGH, both outputs will be HIGH. The latch is then

considered to be in an illegal state in which the outputs labelled Q and $\overline{Q}$ are not complementary. Therefore, as indicated in the state table of Fig. 3.7.1, it is not allowed to have S and R simultaneously HIGH. You may also see that the state of the latch would be unpredictable if R and S, both being HIGH, were to go simultaneously LOW. The final state would depend on which gate is faster.

The RS latch is the basic digital memory element, the building block on which other latches and flip-flops are developed. It also has stand alone applications as a 1-bit memory, for example to store information on single channel analyzer circuits, to capture (identify) very short transient states, or to debounce mechanical switches (due to mechanical spring effects these switches typically make and break contact several times until they reach the final state) . Debouncing is an essential technique in digital circuits. To convince yourself of this, try to count the number of times you actuate a mechanical switch by connecting it directly to a counter input, then do it properly through an RS latch.

EXPERIMENT

RS latches are usually (and conveniently) implemented with gates. Actually, there is only one RS latch in the TTL catalog. Their design may take many forms as illustrated by the Boolean equation for the circuit of Fig. 3.7.1:

$$Q = \overline{R + \overline{Q}} = \overline{R} + (\overline{\overline{S} + Q}) = \overline{R} \cdot (S + Q) = \overline{R}\,S + \overline{R}\,Q = S + \overline{R}\,Q$$

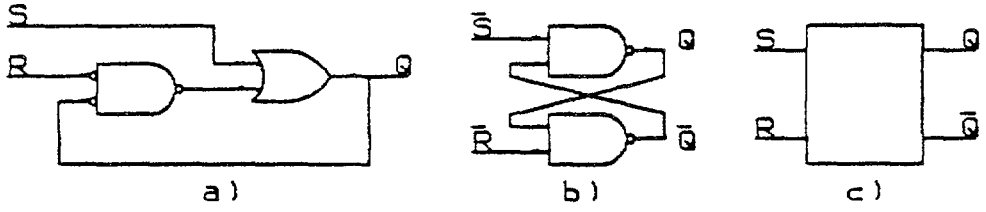
To obtain the last expression we used the substitution $\overline{R}\,S = S$ which is valid in an RS latch because the condition $R = S = 1$ is not allowed to occur. The corresponding circuit is shown in Fig. 3.7.2a (if the $\overline{Q}$ output is also desired, an inverter must be added to the circuit). This is a form particularly useful in the applications: it is written as a sum-of-products and, thus, can be implemented in a PAL device. Another RS latch circuit may be obtained through Morgan's laws:

$$Q = S + \overline{R}\,Q = \overline{\overline{S} \cdot \overline{R}\,Q}$$

The corresponding circuit is shown in Fig. 3.7.2b. This is a most popular form of the latch, made out of two NAND gates. In this form we call it an $\overline{R}\,\overline{S}$ latch and label the inputs $\overline{R}$ and $\overline{S}$ because these variables are now active LOW ($Q = 1$ is obtained with $\overline{S} = 0$, etc.). The no-operation command is now $\overline{S} = \overline{R} = 1$; if we were to draw Fig. 3.7.2b analogous to Fig. 3.7.1, we would place pull-up resistors in both inputs. We will not do so and will, instead, assume that the inputs are always appropriately driven. In Fig. 3.7.2c we represent the latch by a more concise symbol.

Fig. 3.7.2:

RS latch circuits



The state of a latch after power-up is unpredictable. (The same is true for the other latches and flip-flops to be discussed later.) When one wishes to have a known initial state, one must use some kind of power-up set or reset circuit. Such a circuit is shown in fig.3.7.3. A 3-input NAND gate is now used in order to leave the latch's working inputs unperturbed.

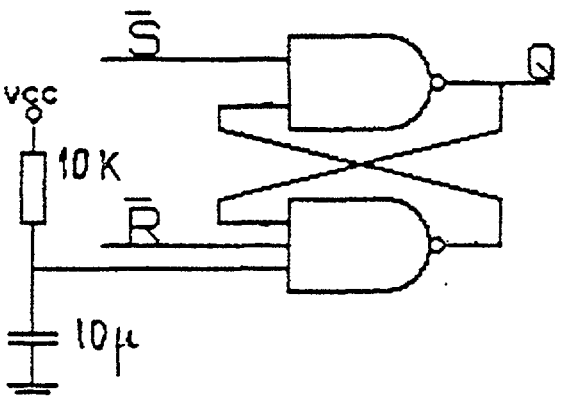


Fig . 3.7.3:

Power-up reset circuit

The gated RS and D latches

A gated RS latch is shown in Fig. 3.7.4a. It is clear that the latch acts as an ungated latch while EN = 1; when EN = 0 no action can take place on the latch. In boolean form this statement reads:

$$Q = (S + \overline{R}\,Q) \cdot EN + Q \cdot \overline{EN}$$

The EN terminal is usually called the ENable input. Referring to the timing diagram of Fig. 3.7.4b, it is usual to designate the state of the latch after the n-1th EN pulse and before the nth pulse by Q_n; the state after the nth pulse and before the $n+1^{th}$, by $Q_n + 1$. (While EN = 1, the output follows whatever is commanded by the S and R inputs. NOTE: Enable in the present context refers to "enable updating of latch". The latching, that is, the retaining mode, is obtained with EN = 0.)

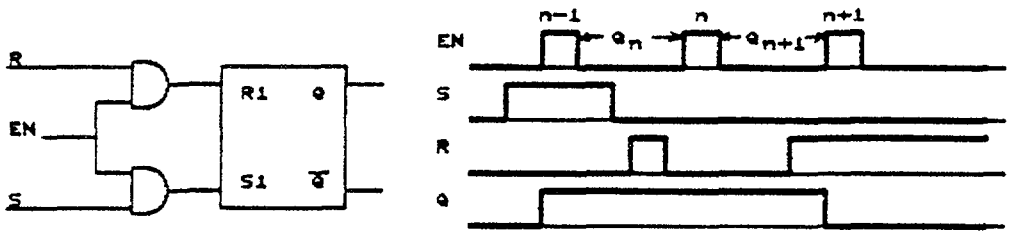


Fig . 3.7.4:

Rs latch circuit and timing diagram.

The enable terminal allows us to use a single input to set or reset the latch. Following convention, we use S as the single input and connect an inverter from S to R. The Q_n state of the latch is then determined by the value of S at the trailing edge of the ENable signal. This configuration of the RS latch is so important in the applications that it deserves a name of its own: the D latch. Here D stands for Delay; the input terminal is labeled D (for Data). Note that $D = S = \overline{R}$; thus, from the RS equation we obtain for the D latch

$$Q = D \cdot EN + Q \cdot \overline{EN}$$

The 74XX373 is one of the most frequently used D-latches. Actually, the 373 is an octal latch, that is, a set of 8 latches activated by a common enable signal. It has the additional feature of tri-state outputs. Another example from the logic catalog is the 74XX75, a quad D-latch.

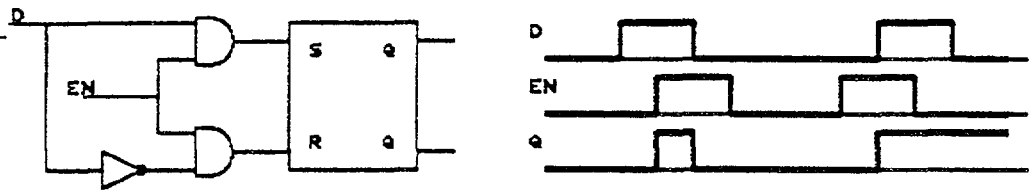


Fig.3.7.5

D latch circuit and timing diagram.

You may use any of the available D latches to see for yourself the fundamental characteristic of latches: their transparency, that is, the output following the input while the latch is enabled. Thus, the data that is latched is the D input data at the trailing edge of the enable signal. This is summarized in Fig. 3.7.5. Of course, one has to take into account the dynamic characteristics (setup and hold times, propagation time) as discussed in Experiment 3.3.

Further to its gated inputs, many latches are enhanced by the addition of ungated inputs that may either set or reset the latch. These are inputs that may be directly connected to the output gates of the latch (to the output NOR gates if the latch is based on a circuit similar to that of Fig. 3.7.1). To distinguish these terminals from the Set and Reset, they usually are given the names PReset and CLear, respectively. They may either be active HIGH or LOW, according to circuit implementation.

The RS and D flip-flops

The transparency of latches implies that whenever the enable input is active, the value that is read from the latch is the value of the D input at the time of reading (disregarding propagation delays). This is inconvenient in many digital systems where memory elements have their inputs connected to the outputs of other memory elements, and where all memory elements are simultaneously enabled. In these systems one typically requires that, each time they are enabled, the elements just respond to the input conditions left after the previous enabling pulse; they should not follow the changes that eventually take place while the circuit is enabled. Flip-flops are the memory elements designed to fulfill this requirement.

There are essentially two ways to design a flip-flop, both using a latch as the basic building block. In one of them the output signal is only allowed to change at the trailing edge of the latch enable input; in the other, an edge detector circuit is introduced in front of the enable input. The first method is pictured in fig.3.7.6. It is clear that when the input labelled CK (ClocK) becomes HIGH the first flip-flop is enabled while the second is disabled due to the inverter in front of EN1.(We reserve the name Enable for the activating input of a latch, and use Clock for the corresponding input of a flip-flop.) The propagation delay through the first latch is enough to ensure that the second latch is disabled before an eventual change occurs in the output of the first. At the trailing edge of the pulse, the first latch is disabled and the second becomes enabled. Only at this time is the output of the flip-flop updated. The propagation time in the second latch ensures that circuits connected to this flip-flop will respond to this updated value only at the next clock pulse. The flip-flop just designed is called a master-slave RS flip-flop. In the logic catalog there are circuits designed according to this principle but corresponding to an extension of the RS state table. They are referred to as JK (master-slave) flip-flops and will be discussed ahead.

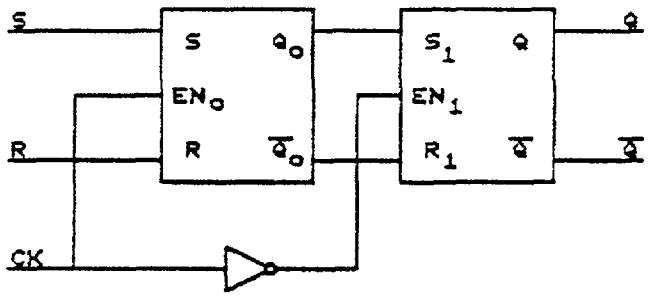


Fig. 3.7.6:

RS master-slave flip flop.

The non-transparency of the flip-flop obtained with the master-slave design allows us to sequentially connect these memory elements. However, there still remains a problem we wish to avoid in many instances. Suppose a situation in which the flip-flop state is Q = 0 and S = R = 0 so that no change should occur in the flip-flop output. At any time while the clock is HIGH a glitch or other undesired noise signal appearing at the S input may be able to set the master latch, and the flip-flop will be updated to a false value at the end of the clock pulse. Such a situation is avoided if the second scheme to build a flip-flop is used. This scheme is represented in Fig. 3.7.7. It is clear that the CK pulse will produce in the edge detection circuit (see Experiment 3.3) a very narrow pulse, the width of which is roughly equal to the propagation time of the inverter. Thus, the RS latch will be enabled only at the rising transition of the CK pulse. It is clear that any changes on the S or R inputs occurring after the rising edge of the clock pulse will have no effect on the flip-flop output. These types of flip-flops are called edge-triggered. Both positive (rising) and negative (falling) edge-triggered flip-flops are available in the logic catalog.

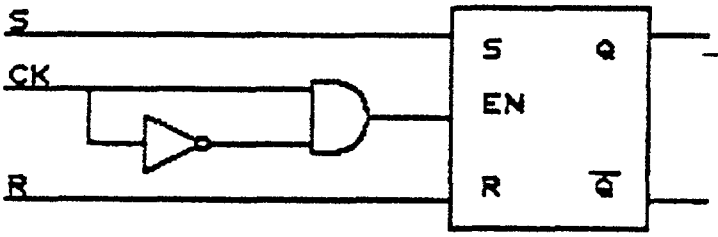


Fig.3.7.7

Positive edge triggered flip flop.

The D-type positive edge-triggered flip-flop is one of the most commonly used flip-flops. Well known examples are the 74xx74, which contains two independent flip-flops, which is an octal flip-flop (8 flip-flops activated by a common clock pulse) with tri-state outputs. Again we emphasize that the different timing characteristics of latches and flip-flops should be clearly understood. As an exercise observe these differences with the 373 D latch and the 374 flip-flop.

The circuit of Fig. 3.7.7 shows clearly the principle used to obtain an edge-triggered flip-flop. However, such a circuit depends critically on the rise time of the clock pulse. A different implementation of the same principle is used in the available integrated D flip-flops. The logic diagram of the 74XX74 is shown in Fig.3.7.8.

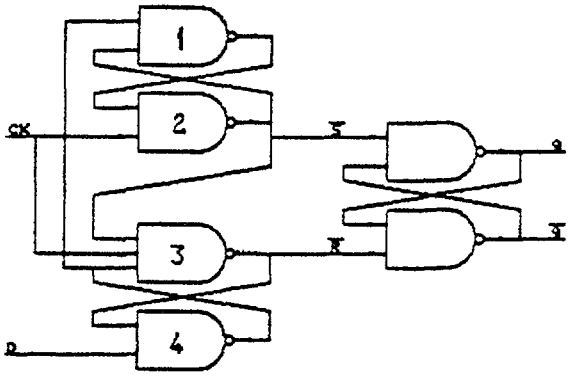


Fig.3.7.8:

74xx74 D-type flip flop logic diagram.

To follow the operation of this circuit consider the case in which $Q_n = 0$ and D = 1. Note that while CK = 0 both $\bar{S}$ and $\bar{R}$ are HIGH. With D = 1 and

$\overline{R}$ = 1 the output of gate 4 is LOW; this ensures that $\overline{R}$ stays HIGH when CK becomes HIGH. Gate 1 will be HIGH and gate 2 will go LOW with the rising edge of CK; this will set the flip-flop to state Q = 1. Because $\overline{S}$ is also applied to gate 3, this guarantees that $\overline{R}$ stays HIGH. If now D goes LOW (with CK still HIGH) no change is produced on the Q output: gate 4 changes but it no longer affects the outputs of gates 2 and 3. Thus, in the case considered, the circuit behaves as a positive edge-triggered flip-flop. You may verify that the same applies to the other possible cases. It is also clear that the output of the flip-flop is updated at the rising edge of the CK signal; the internal delay of the flip-flop will prevent similar flip-flops connected to it to respond to the updated value. You may check this using the two flip-flops of the 74 package.

The JK flip-flop

The RS state table is displayed again in Fig. 3.7.9. It is clear that to obtain the most general form of flip-flop one requires the command 11 to produce $\overline{Q}_n$: then all possible cases (to become 0 or 1, to change or not to change whatever the previous state is) are included in the state table. The device that implements such a state table is called a JK flip-flop; its table is also shown in Fig. 3.7.9.

Fig.3.7.9:

State tables for RS and JK flip flops.

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	forbidden

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

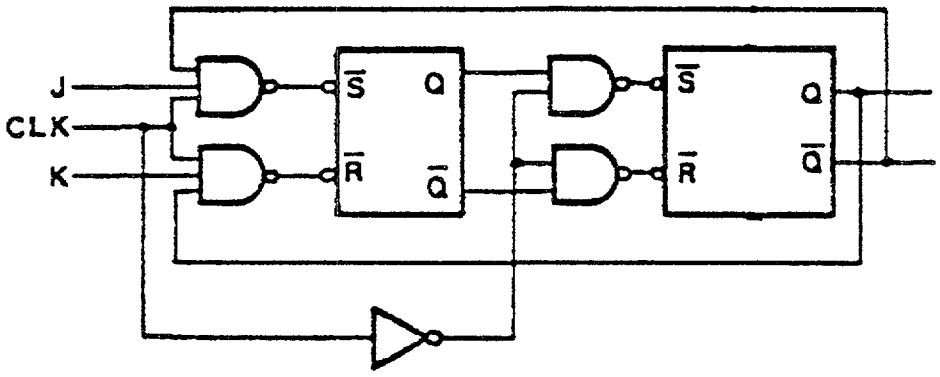
From this table we may easily write the boolean equation for the JK flip-flop:

$$Q_{n+1} = \overline{J}\,\overline{K}\,Q_n = J\,\overline{K} + J\,K\,\overline{Q}_n = \overline{J}\,\overline{K}\,Q_n + J\,\overline{K}\,Q_n + J\,\overline{K}\,\overline{Q}_n + J\,K\,\overline{Q}_n = J\,\overline{Q}_n + \overline{K}\,Q_n$$

A suitable logic diagram, close to that of the 74LS76 circuit, is shown in Fig. 3.7.10. This is a master-slave type of structure. You may easily check that it conforms to the state table of the JK flip-flop. This circuit is said to be pulse triggered. This is supposed to indicate that the output is updated at the trailing edge of the clock pulse and that it is affected by the input values at the leading edge of the clock or while the clock is active (as discussed for the RS master-slave flip-flop).

Fig.3.7.10:

Master-slave JK flip flop.



The JK may also be implemented with edge-triggered flip-flops (either rising, positive or falling, negative edge). Such a flip-flop is edge-sensitive; it is not affected by changes that may take place at the inputs after the active edge of the clock pulse. The 74XX109 is an example of a positive edge-triggered flip-flop; the 74XX112, of a negative edge-triggered one. Both of these flip-flops have asynchronous preset and clear inputs.

As seen from the state table of the JK flip-flop, if one is just interested in the toggle/no toggle operation of the flip-flop, one forces J = K. A device connected in this way is called a T-type flip-flop (from Toggle). Such flip-flops are frequently used in counter circuits, as discussed in a later experiment. There are no T flip-flops in the logic catalog.

A critical point in the use of flip-flops is the correct understanding of their timing relations. An exercise designed to clearly show the differences between the various types of available flip-flops, as well as between latches and flip-flops, is an instructive and important one. A simple pulse generator, complemented with a couple of monostable circuits, is able to provide all the signals required for the proper observation of the timing relations in a scope.

Transition tables

The operation of flip-flops has been described by state tables. The transition tables provide an alternate description which is frequently more convenient to use. Both tables are shown in Fig. 3.7.11 for the JK flip-flop, which includes all other flip-flops as particular cases. For reference, the figure also includes the boolean equations of the various flip-flops.

The transition table is easily derived from the state table. For example, a 0 0 transition is obtained with J = 0 and K = 0 (for $Q_n = 0$) or J = 0 and K = 1 (whatever the value of Q_n is); thus K may have any value (we may call it a don't care value) but J must be 0. Transition tables are particularly useful in the systematic design of sequential circuits.

		J K	Q_{n+1}	transition	J K
R S:	$Q_{n+1} = S + \overline{R}\,Q_n$	0 0	Q_n	0 → 0	0 x
D:	$Q_{n+1} = D_n$	0 1	0	0 → 1	1 x
J K:	$Q_{n+1} = J\,\overline{Q}_n + \overline{K}\,Q_n$	1 0	1	1 → 0	x 1
T:	$Q_{n+1} = T\,Q_n + \overline{T}\,Q_n$	1 1	$\overline{Q}_n$	1 → 1	x 0

Fig.3.7.11

State and transition tables and Boolean equations for flip-flops.

Notes:

Experiment 3.8

COUNTERS AND SHIFT REGISTERS

OBJECTIVE

The objective of this experiment is to demonstrate the properties and performance of counters and shift registers and to become acquainted with their main representatives in the logic catalog.

REVIEW

Flip-flops and latches have been discussed in a previous experiment. Here we will see how they are assembled in circuits designed to perform well designed tasks, such as binary counting and data shifting. Many important, basic circuits of counters and shift registers are available in integrated circuit form and we will get acquainted with their main types. Timing diagrams are essential to accurately describe the dynamic behaviour of these circuits and will be used extensively. The waveforms which they represent may be observed with a scope, or a logic analyzer.

Large scale integrated counters are dealt with in a separate experiment

Asynchronous binary counters

The logic diagram of a 4 bit binary counter is shown in Fig. 3.8.1. All of the 4 T-type flip-flops have their T inputs at logic level 1; thus, all flip-flops will toggle each time there is a HIGH to LOW transition on their clock inputs. The counter is initialized to an all zero condition by applying a pulse to the common clear line, $\overline{CLR}$. As shown in the timing diagram of Fig. 3.8.2, the first pulse on the CLK line will toggle the A flip-flop and Q_A goes HIGH. The second pulse on the CLK line will toggle it again and, as Q_A goes LOW, the B flip-flop is toggled. The further actions shown in the timing diagram are explained in a similar way.

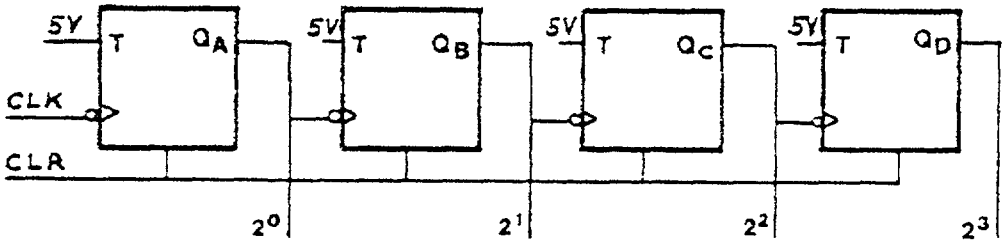
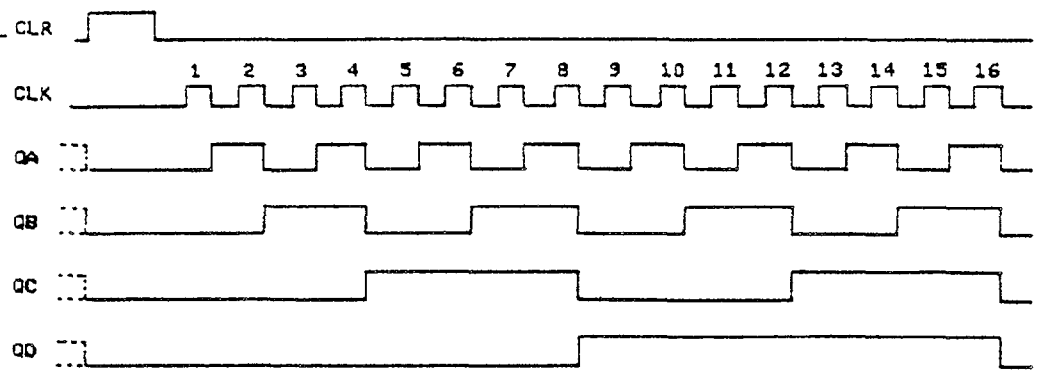


Fig.3.8.1

4 bit asynchronous binary counter

Fig. 3.8.2:

Binary counter timing diagram.



Each flip-flop in the counter has a binary weight associated with it. The first flip-flop (to which the external pulses are applied) has a weight 2^0, the next one 2^1, etc. Thus the number of counted CLK pulses is, in binary code, $Q_DQ_CQ_BQ_A$. The counting sequence is clearly seen in the timing diagram: the binary contents of the counter is 0 before the first pulse, becoming 1 after the first pulse, 2 after the second, etc. After the 16^{th} CLK pulse the circuit overflows, going back to the all zero state. For this reason, the circuit is also called a modulo-16 counter. Of course, the HIGH to LOW transition of Q_D can be used as CLK input to another, identical counter to form a modulo-256 counter. Two independent 4 bit asynchronous binay counters are available in a 16 bit package, type 74XX393; the corrsponding single counter is type 93.

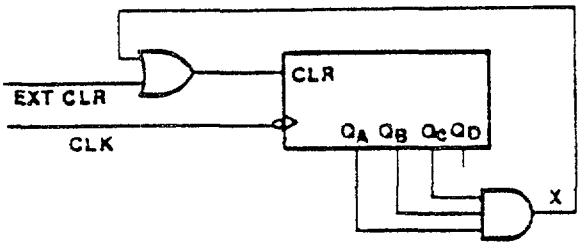
The timing diagram of Fig. 3.8.2 is not detailed enough to show the propagation delays along the counter. As an exercise, measure the propagation delay from the input to the last flip flop, and try a similar measurement for the propagation through a single flip flop. The fact that various flip flops are not simultaneously updated in asynchorous counters must always be kept in mind.

Modulo-n counters; BCD counters

Using digital feedback it is possible to implement modulo-n counters with n different from a power of 2.(The number N of required flip-flops is such that $n<2^N$.). For instance, the circuit of fig.3.8.3 will form a modulo-7 counter. As can be seen from the timing diagram of fig.3.8.4, after the 7th CLK pulse,U $Q_A=Q_B=Q_C=1$ and so the X line will go HIGH clearing all the flip-flops back to the all zero state. Note that this implies that X will be HIGH for a time long enough to clear all the counter flip flops. With the circuit shown this may not be the case. (The timing diagram was drawn, following tradition, with pulses applied to the CLK input at a constant rate. Of course, pulses may arrive randomly in time and, in nuclear pulse counting, they will certainly do.)

Fig. 3.8.3:

Modulo-7 counter



A typical application of modulo-n counters is frequency division. For example, a stable microprocessor crystal controlled clock is divided down to generate time marks to be used in serial data communication. In this case, the input to the counter is a pulse train of frequency f and the aim is to obtain another pulse train with frequency f/n.

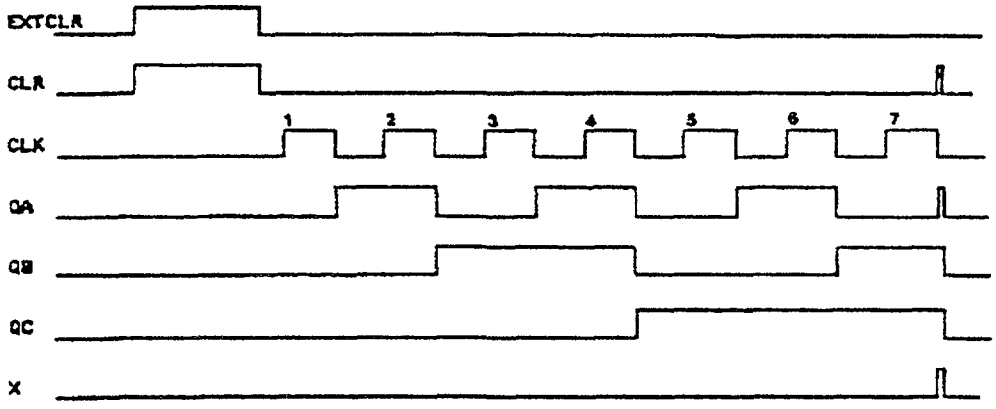


Fig. 3.8.4:

Timing diagram for modulo-7 counter.

Binary coded decimal counters, usually called BCD counters are modulo-10 counters. The logic diagram of the 74XX90 integrated asynchronous decade is shown in Fig.3.8.5, The 74xx390 is identical to this but with two independent counters per package. It is seen that one flip-flop is separated from the group of the other three, which is organized as a modulo-5 counter. Thus the decade may work in two different modes of operation, called the BCD and the bi-quinary modes.

We first refer to the modulo-5 counter. Notice the gate connections at the clock inputs of the B and D flip-flops. The signals there applied follow the equations $CLK_B = Q_A \cdot \overline{Q_D}$ and $CLK_D = Q_A \cdot (\overline{Q_B} \cdot \overline{Q_A} + \overline{Q_C} \cdot \overline{Q_D})$. Thus the B flip-flop will only toggle while $Q_D = 0$ (that is,until the arrival of the 4th pulse at BIN); and flip-flop D will only toggle with signals that arrive at B_{IN} when either $Q_B = Q_C = 1$ or $Q_D = 1$. This assures a modulo-5 counting sequence as is clearly shown in Fig. 3.8.6 (note that the Q_A line is the clock line for this counter). Notice that Q_D is HIGH during the time interval between two clock pulses and that the highest state in the modulo-5 counter is $Q_D = Q_C = Q_B = 100$. Unlike the circuit shown in Fig. 3.8.3, this circuit behaves reliably. The 5th incoming pulse just forces the return to the initial all zero state. The HIGH to LOW transition in Q_D may be used to clock another flip-flop.

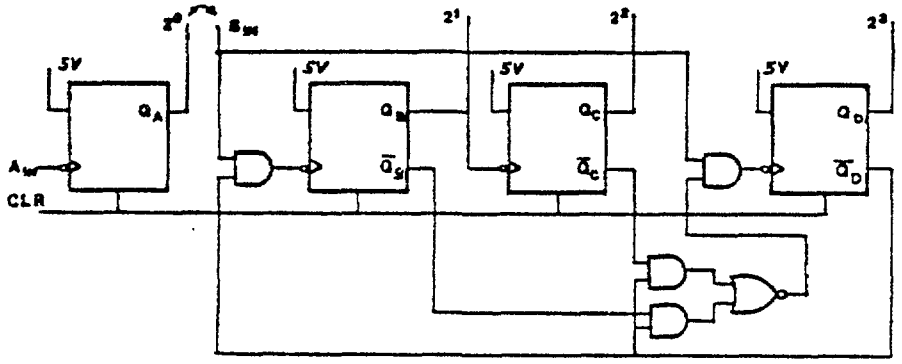


Fig. 3.8.5:

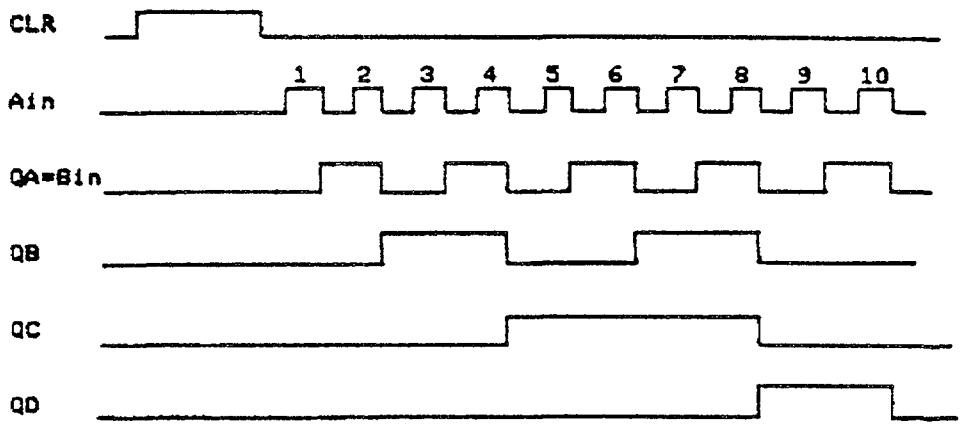
Decade counter (74xx90).

In the BCD mode, the Q_A output is connected to B_{IN}. You may verify that the binary number $Q_D Q_C Q_B Q_A$ then represents the number of pulses counted, justifying the name BCD (Binary Coded Decimal).

In frequency division applications it is sometimes better to have such a symmetrical, 50% duty cycle output. In the bi-quinary mode of operation, the input signal is applied to B_{IN} and Q_D is tied to A_{IN}; Q_A gives the symmetrical output.

Fig. 3.8.6:

BCD counting sequence



Look at the waveforms of both operating modes of the 74xx90 (or 390) on an oscilloscope and determine the propagation time though this asynchronous mode.

Timing problems with asynchronous counters

The internal propagation delays of each flip-flop in an asynchronous counter may cause errors when logic decisions based on the counter contents are taken. This is due to transient intermediate states that exist during just a few nanoseconds. Narrow as they may be, these glitches (spikes) may trigger undesired events elsewhere in the system. As an example, assume that in the circuit of Fig 3.8.7, some decision is to be taken when both Q_A and Q_B are LOW. The table presented on the following page, shows various states that the counter switches through when pulses are coming. The intermediate states, shown in brackets, occur because each flip-flop toggles only after the previous one goes from 1 to 0. Some of the intermediate states generate spurious states at the output of the NOR gate. Some of these are harmless, others may cause serious problems, as the diagram of Fig. 3.8.8 emphasizes. The gliches can be avoided simply by using synchronous counters as discusses earlier. However, if the asynchronous counters are to be used in a digital system, the design must guarantee that any logical decision based on their outputs is postponed until all the spurious intermediate states have been crossed. For the example under discussion, a simple circuit modification, shown in Fig. 3.8.9, will do the job. The circuit works as follows.

Fig. 3.8.7:

Incorrect decision logic

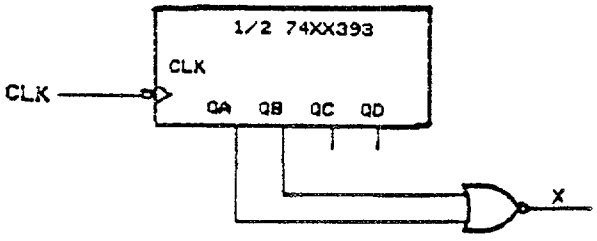


Fig. 3.8.8:

Glitches in asynchonous counters.

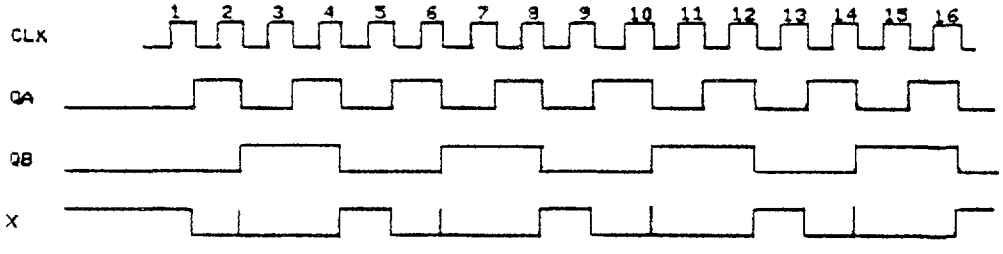


Table 3.8.1: Switching states of a counter

		Q_D	Q_C	Q_B	Q_A	Output x
		0	0	0	0	0
After pulse	1	0	0	0	1	0
	(	0	0	0	0)	*
	2	0	0	1	0	0
	3	0	0	1	1	0
	(	0	0	1	0)	0
	(	0	0	0	0)	*
	4	0	1	0	0	
	5	0	1	0	1	1
	(	0	1	0	0)	*
	6	0	1	1	0	0
	7	0	1	1	1	0
	(	0	1	1	0)	0
	(	0	1	0	0)	*
	(	0	0	0	0)	*
	8	1	0	0	0	1
	9	1	0	0	1	0
	(	1	0	0	0)	*
	10	1	0	1	0	0
	11	1	0	1	1	0
	(	1	0	1	0)	0
	(	1	0	0	0)	1
	12	1	1	0	0	1
	13	1	1	0	1	0
	(	1	1	0	0)	*
	14	1	1	1	0	0
	15	1	1	1	1	0
	(	1	1	1	0)	0
	(	1	1	0	0)	*
	(	1	0	0	0)	*
	16	0	0	0	0	1

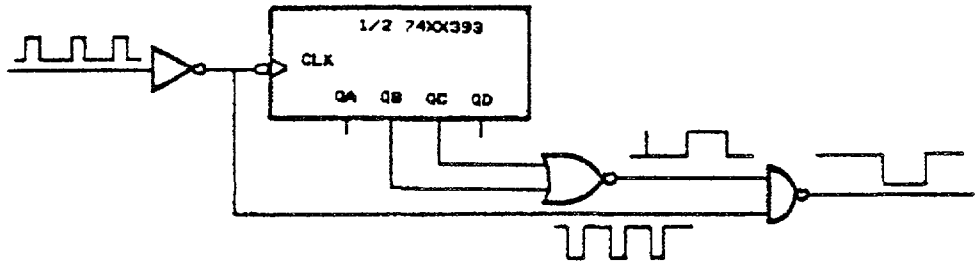
By inverting the incoming clock pulses, all the toggling within the counter will follow the leading egde of the pulse. During the time equal to the width of the incoming pulse, any desicion is inhibited by the NAND gate. None of the glitches coming out of the NOR gate will pass this, and only a stable condition $Q_A = Q_B = 0$ will be honored. The output signal will be slightly shorted, but this is of no consequence.

It is instructive to check the operation of this circuits or of another similar one serving the same purpose.

Glitches due to asynchronous counting are also easily observable in the output of code converters. Connect the 90 decoder to the 74xx42 BCD to 10-line converter, and observe

Fig. 3.8.9:

Eliminating glitches.



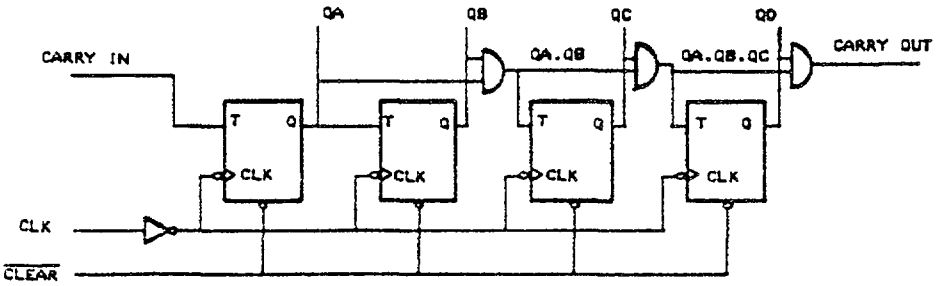
the 42 outputs. You will conclude that any flip flop connected to these outputs will be triggered erroneously, due to the asynchronous nature of the counter.

Synchronous counters

Asynchronous counters are sometimes called ripple-through counters, a name derived from the fact that one can actually see the information ripple through the various stages of the circuit. This is not so in synchronous counters where the same clock signal is applied simultaneously to all flip-flops. In this case, the decision whether a certain flip-flop is to toggle or not must be prepared in advance, based upon the present state of all the flip-flops. An example of a synchronous counter based on T flip-flops is shown in Fig. 3.8.10.

Fig. 3.8.10:

Synchronous counters.



If the CARRY IN input is HIGH, as it will normally be if this is a single counter or the first in a cascade of counters, the first flip-flop will toggle with every clock pulse. The toggling takes place at the rising edge of the incoming pulse because the pulse is inverted before it reaches the CLK input of the various flip-flops. The second flip-flop only toggles when $Q_A = 1$. The third toggles when $Q_A = Q_B = 1$, a condition determined by the AND gate; and the other stages follow similarly. A CARRY OUT signal is generated when all flip-flops are in state 1; this is the signal that is required as CARRY IN for the next IC if a cascade of several counters is being used.

The timing diagram of the above synchronous counter is shown in Fig. 3.8.11. Apart from the very small differences in the internal propagation times of the various flip-flops, all transitions take place simultaneously. However, as you may already have realized, for a cascade of such counters this CARRY IN/CARRY OUT scheme actually leads to a ripple-through operation from one counter to the next one. For very fast counting more sophisticated techniques, such as CARRY-LOOK-AHEAD, are required.

Note that the correct behaviour of this type of circuit rests upon the dynamic characteristics (see Experiment 3.3) of the edge-triggered flip-flops used. For example, the second flip-flop does not toggle with the first clock pulse because, when the state at its T input is sampled (at the rising edge of the clock), Q_A is still LOW; and it remains LOW while the signal propagates through the first flip-flop, an interval that exceeds the hold time requirement.

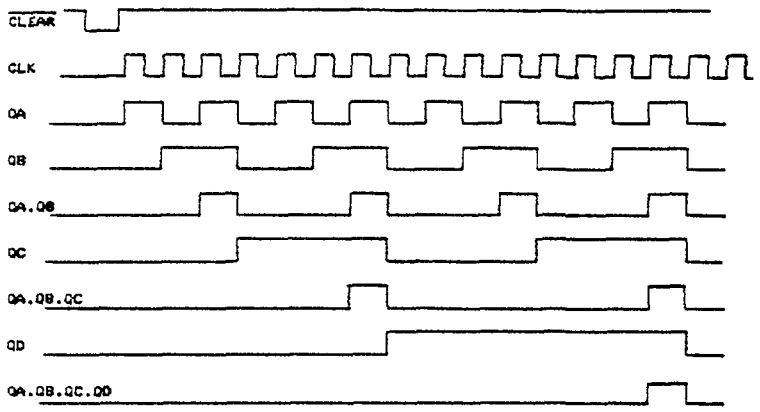


Fig. 3.8.11: Synchronous binary counter sequance.

In the synchronous counter of Fig. 3.8.10, the $\overline{\text{CLEAR}}$ signal acts asynchronously, that is, independently of the clock signal. This is how the 74xx161 counter behaves. Some other IC counters have a synchronous CLEAR, that is, the flip-flops are cleared to zero only at the active edge of the first clock pulse after $\overline{\text{CLEAR}}$ becomes LOW ; as, for example, in the case of the 74XX163 counter.

The above counters also have another enhancement, called parallel load. The counters may be set to a selected value by a control signal, $\overline{\text{LOAD}}$. Again, this operation may take place synchronously (as in the 74XX163) or asynchronously (as in the 74XX193). The circuit used to control and parallel load of this counter is represented in Fig. 3.8.12. You may easily see how it operates.

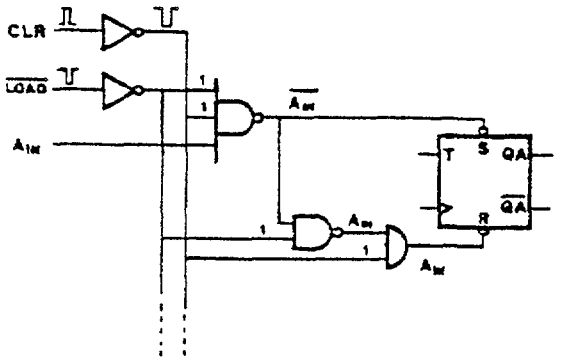


Fig. 3.8.12: Parallel load and clear circuitry.

Another enhancement now available with many types of integrated counters is the tri-state output feature. As discussed elsewhere, this is very useful feature when the counter outputs are to be connected to a bus. There will be then no need to use additional circuits for bussing purposes. Examples of these counters are the type numbers 74XX69X.

As an exercise, use one of the synchronous counters together with the 42 code converter, and verify that there are no glitches on the 42 outputs. Check also the ripple-through nature of the CARRY IN/CARRY OUT scheme.

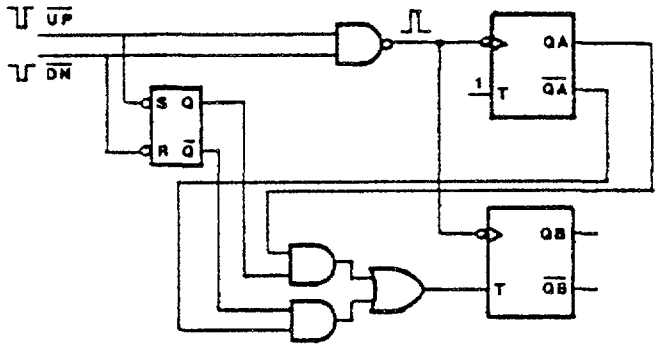
UP/DOWN counters

Some of the available IC synchronous counters can be made to either count up or count down. This is implemented in two different ways. In one of them a single clock input is used and the counting mode is selected through an up/$\overline{\text{down}}$ input. In the other, illustrated in Fig.3.8.13, separate clock inputs are used for up and down counting. The circuit is taken from the 74XX193 counter. It is seen that the up/down decision is made with a simple

$\overline{R}\,\overline{S}$ flip-flop. If it is an $\overline{UP}$ pulse, Q goes HIGH and Q_A is applied to the T input of the B flip-flop. This is what is needed for up counting. If it is a DOWN pulse, $\overline{Q}$ goes HIGH and $\overline{Q}_A$ is applied to the input of the B flip-flop. This is what is needed for down counting because B must toggle when A goes from 0 to 1.

Fig. 3.8.13:

Up/down counting circuit.



These integrated counters are sophisticated circuits and one must read the information available in the data book carefully. One must be aware of such difficulties as, for example, the fact that, if one applies practically simultaneous signals to both clock inputs of a 74XX193, errors will certainly occur.

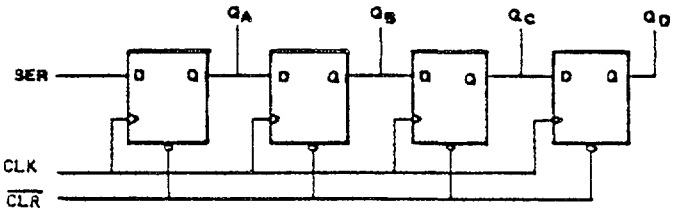
An interesting application of the up/down counters is in tracking analog-to-digital converters. In these converters, the input signal is compared to the output of a digital-to-analog converter driven by the up/down counter. The comparator output controls whether the counting is up or down. Try to design the appropriate schematic in detail.

Shift registers

Shift registers are made of a series of interconnected D-type edge triggered flip-flops. The data is input in a serial or, in some of the available IC types, in a parallel mode. Similarly, the output data is available serially and, for some IC types, in parallel. A typical circuit for a serial in/parallel out shift register is shown in Fig. 3.8.14 and the corresponding timing diagram in Fig. 3.8.15. The diagram clearly shows the circuit operation. Every clock pulse shifts the data present in each flip-flop to the one to its right. Type 74XX164 is an 8 bit shift register which works in a similar way.

Fig. 3.8.14:

Serial in/ parallel out-shift register



More sophisticated registers are available in the logic catalog. For example, the 74XX194 is a 4 bit parallel in/parallel out bidirectional shift register with synchronous load and asynchronous clear.

Shift registers find applications in sequential memories, serial to parallel and parallel to serial data conversion, and digital delay lines.

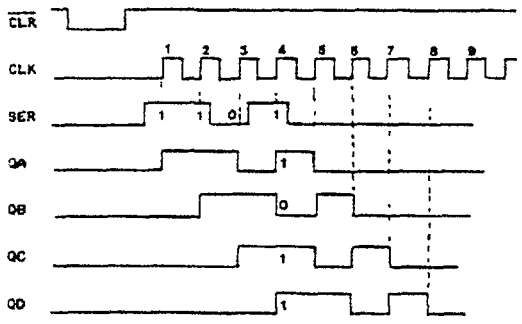


Fig. 3.8.15:

Shift register timing diagram

As an example, design and test an n-bit switchtail (Johnson) counter. This is made by connecting the complemented output of the last, n^{th}, flip flop to the input of the first one.

If you use the 74xx164 shift register, an external inverter is required to complement the flip flop output. Try first a 3-bit counter. Before testing it, write a table showing the state of the counter as the function of the counter pulses (that is the value of $Q_2Q_1Q_0$ for each value of the counter content). Note that in this counter only one bit changes when the counter moves from one state to the next. This ensures glitch-free operation of decoding circuits; see the data sheet of the 74HC4022 counter.

As another exercise, design a ring counter, using the 194 register. In a ring counter, the non-complemented output of the last flip flop is connected to the input of the first one. Use the parallel load capability of the 194 to reset the counter to zero. This value will be represented by the $Q_3Q_2Q_1Q_0 = 0001$ state. The state representation of the counted values 1 to 3 is selected to be compatible with shift-write operation.

Pseudorandom bit sequence generators are used, for example, to produce random noise or random time signals. They can be made simply by connecting, for example, the output of the last two flip flops of a n-bit shift register to an EXCLUSIVE-OR gate, and the output of this gate to the shift register input. The register must be initialized to a non-zero value. (or make $D_0 = Q_2 + Q_3 + Q_0 + Q_1 + Q_2 + Q_3$ and don't care about initialization). Select an appropriate 4 bit register, and determine the complete sequence. Of couse, you may have a much larger sequence if you increase the size of the register.

Notes:

Experiment 3.9

LSI COUNTERS

The objective of this experiment is to get acquainted with LSI counters, and to assemble and test a complete scaler with 4-digit display.

OBJECTIVE

The MM74C925 is an LSI 4-digit counter. As shown in Fig. 3.9.1 the circuit includes an internal output latch for its 4 decades and multiplexing circuitry to present succesively each decade to the internal BCD to 7-segment decoder. NPN output drivers connect the decoder to the outside world. The decade that is currently being decoded is identified by raising 1 out of 4 output control lines.

REVIEW

A complete 4-decade scaler, with a 4-digit display and input gate control, desinged around the 925, is to be assembled and tested in this experiment.

The 925 is just an example of LSI counter. Another example is the Intersil 7031 which is used in some commercial scalers (see TECDOC-426).

The diagram of the circuit to be assembled is shown in Fig. 3.9.2. The component location on the prepared circuit board is shown in Fig. 3.9.3.

EXPERIMENT

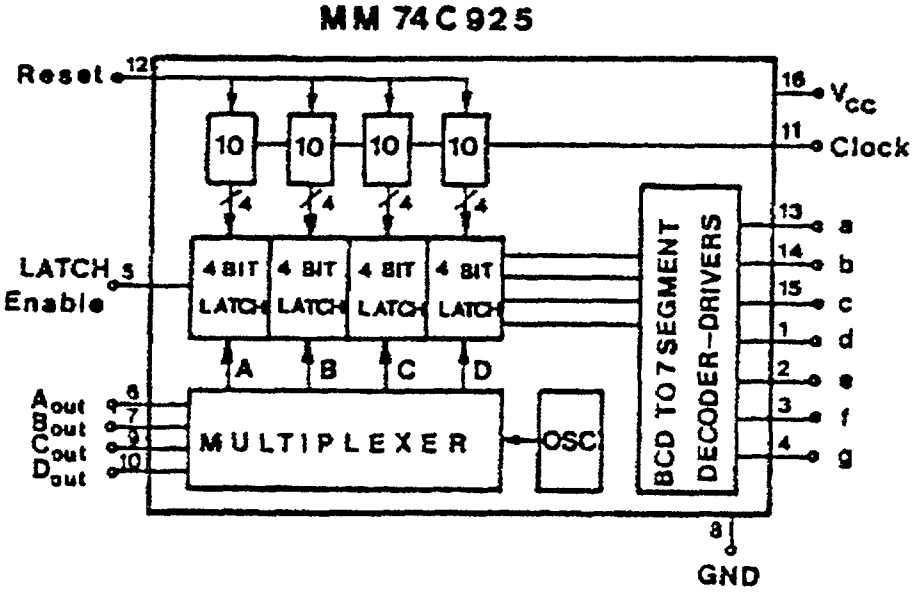


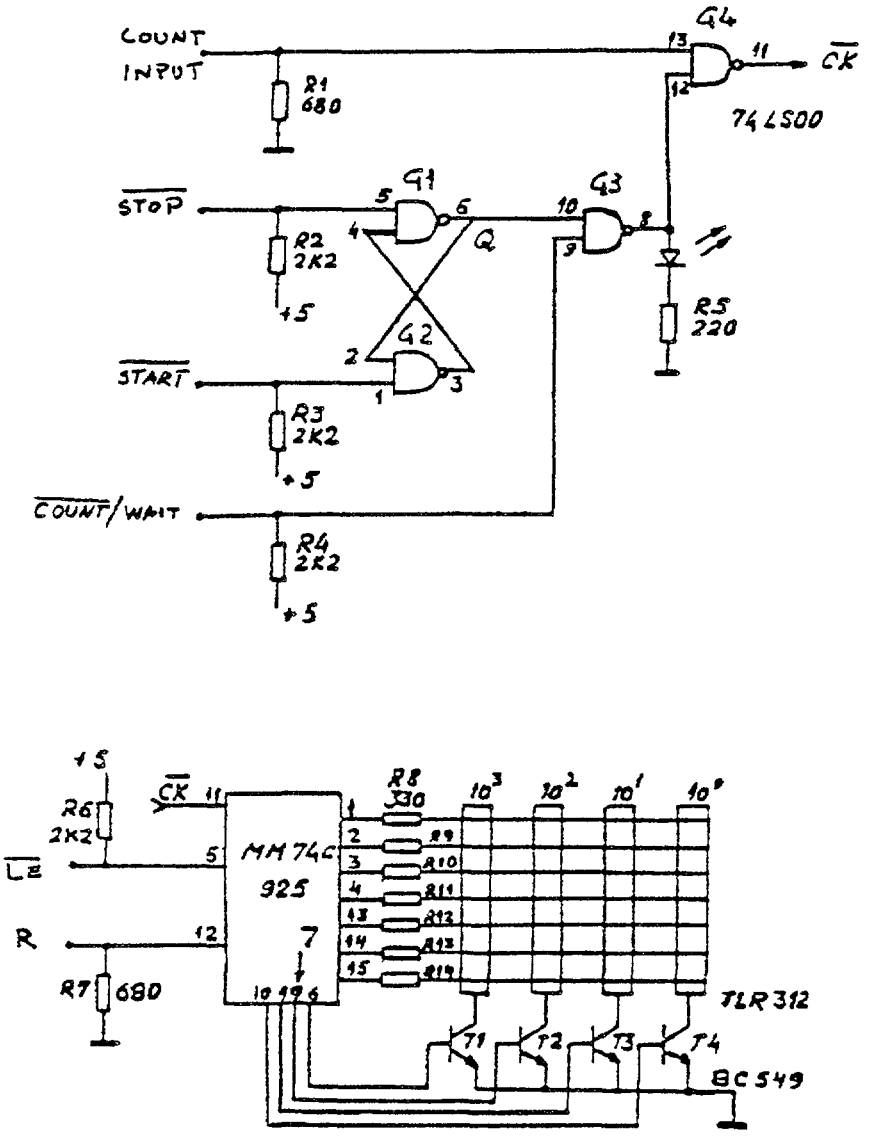
Fig. 3.9.1: Logic and block diagram of the MM74C925

We refer first to the input gate circuitry which is built using a single 74LS00 NAND gate package. G4 acts as the count input gate. This gate is under the control of G3 which is itself controlled by theCOUNT/WAIT line if its other input (pin 10) is in state 1. In this condition, the input gate will be closed while this line is in state 1. Gates G1 and G2 are interconnected as an R S flip-flop; thus a negative edge applied the input is enough to set the Q output (pin 6) to logic 1 and a negative edge at the STOP input is enough to reset the Q output to logic O. Therefore, to use the COUNT/WAIT input to control the input gate, one must first set the Q output (and thus pin 10 of G3) to logic 1. If the COUNT/ WAIT input is left unused, pin 9 of G3 will be at logic 1 and the input gate control is performed by the flip-flop. In summary, the input gate may be controlled either by a level (applied to the COUNT/ WAIT input) or by negative going transitions (applied to the START or the START inputs).

The LED digit displays are of the common-cathode type. Transistor switches are used to

Fig. 3.9.2:

Circuit diagram of a 4-decade scaler



connect the common-cathode of each individual digit to ground; only one digit will be on at any single time. The switches are actuated by the A_{out} to D_{out} output lines of the 925, the A_{out} line corrresponding to the most significant digit and the D_{out} line to the least significant. The oscillator that advances the multiplexing circuitry, and the related output control lines, is also internal to the 925; these lines are advanced at a frequency of 1 kHz

and to the human eye the digits appear to be continuouslyis lit. You may use a scope to check the frequency, and verify that only one transistor at a time is conducting.

The 4 LED 7-segment digits are all connected to a 7-line bus driven by the 925; the 330R resistors are used to limit the current to each segment (and thus the power dissipation on the 925). The bus is time shared by the four digits; the information on the bus at any one time pertains to the decade that is being displayed. You may used a scope triggered by one of the output control lines A_{out} to D_{out} to verify that, if different numbers are shown on the various digit, some of the segments change state when the display is advanced to the next digit (adjust the scope sweep time to show information pertaining to the 4 digits on the screen with the most significant digit on the left).

The scaler is cleared by a pulse applied at the R (reset) input. The contents of the 4 decades may be latched by using the $\overline{LE}$ input; while $\overline{LE}$ = 0, the display shows the contents of the decades at the time of the 1 → 0 transition on the $\overline{LE}$ input (ignoring propagation time). The counting is not affected by the latching operation. The minimum guaranteed pulse widths for valid operation at the $\overline{LE}$ or R inputs is 250 ns (typical values can be shorter than 100 ns).

You may verify that the counter advances on the positive edge of the count input (the 925 itself advances on the negative edge of its $\overline{CK}$ input). The maximum guaranteed counting rate is 2 MHz.

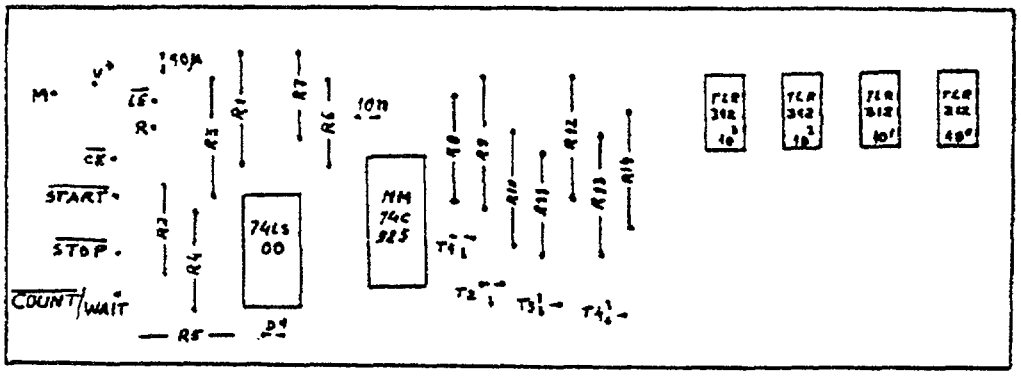


Fig. 3.9.3: Component location on the PCB of the 4-decade

Notes:

EXPERIMENT 3.10

MEMORIES

The objective of this experiment is to discuss memories, their organization and the ways in which they are accessed.

OBJECTIVE

A memory is a device that stores binary information in groups of bits called words. A word is defined as an entity that is written to or read from memory as a single unit. A control signal is required to specify the direction of information flow, that is, whether the information is to be stored (memory write) or retrieved (memory read). Some memories require an already decoded signal: they are controlled by two lines, usually labelled !WR and !RD in IC memories.

REVIEW

Memories may be classified according to access mode into random access and sequential access memories. An example of the latter, made out of shift registers, is shown in Fig.3.10.1. Such a memory is used, for example, in logic analyzers (see Experiment 3.11). Examples of sequential memories implemented in other physical systems are floppy disks and magnetic tapes. The characteristic feature of a sequential memory is that the words are written and read in sequence. In the memory of Fig.3.10.1, a word that is presently on bit 0 of the registers is only accessed after M-1 bits have been read (that is, made available at the register outputs). This particular sequential memory is called a FIFO (First In First Out) memory because, if one starts from an initially cleared memory, the first word that is written (in) is the first to be read (out). As an exercise, you may design, again using shift registers, a sequential memory of the FILO (First In Last Out) type. Sequential memories are particularly useful when the stored data is to be read either in the same order (FIFO) or in inverse order (FILO) as they have been written.

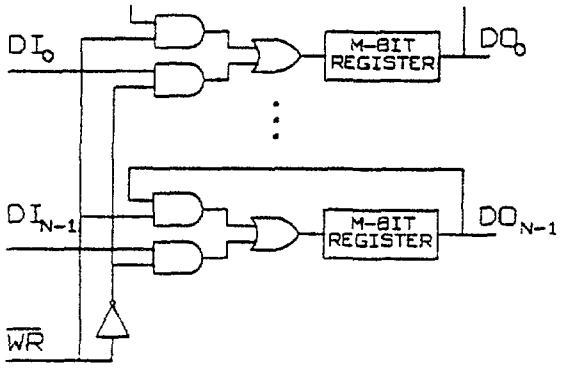


Fig. 3.10.1: Sequential memory of M words of N bits.

In a random access memory (RAM), the location where the word resides in memory is selected by an address register. An n-bit register can specify 2^n words and is set according to the state of n address lines (for example, 10 lines, A9...A0, for a 1K memory). Thus, a word is selected immediately,independently of its location. The access time, that is, the time required to select a location and then write or read it, is the same for every location.

RAMs are physically organized as a matrix of memory cells. Each cell may be a flip-flop (as in the case of static RAMs) or just a capacitor (as in the case of dynamic RAMs). With the latter, some special circuits must be provided to periodically refresh the memory, that is, read its contents and recharge the capacitors associated with one of the logic states (the capacitors are always discharging through leakage paths). These dynamic RAMs are simpler, and therefore able to have higher bit densities than static RAMs. Dynamic RAMs with integrated refresh circuitry are also available; they are appropriately called pseudo-static RAMs because the refresh circuitry is transparent to the user. Dynamic RAMs are generally organized as NX1 memories, with values of N up to 1M commercially available at the present time. For a 256KX1 memory, for example, 18 address lines are required; this is a large number, and the memory ancillary circuits are designed to receive the address bits in a multiplexed manner, 9 bits at a time, with two signals, usually labelled !CAS and !RAS controlling the process (CAS and RAS are acronyms for Column and Row Address Select; the bits are physically arranged as a matrix, and each one is selected through the simultaneous selection of its column and row). Dynamic RAMs are typically used in computers where large memories are required.

Static RAMs are mostly organized as memories of N words of 8 bits; with this structure they are usually called byte-wide memories . For example, 8K byte RAMs are frequently used in microprocessor controlled systems. An N word memory requires n address lines ($2^n = N$); in static RAMs these usually connect to n input pins. A further address related pin is available; this is usually labelled $\overline{CS}$ (from Chip Select). The $\overline{CS}$ input allows for memory expansion. For example, consider that an 8K byte memory is to be made out of 8 byte-wide chips of 2K words. The 11 address lines A10-A0 form a bus to which all the memory chips are connected. The remaining 2 lines necessary to address the 8K space, A12-A11, are to be separately decoded to select one of the chips at a time. The chip selection logic is most frequently designed around a 74XX138 decoder; a circuit for the case just described is shown in Fig. 3.10.2.

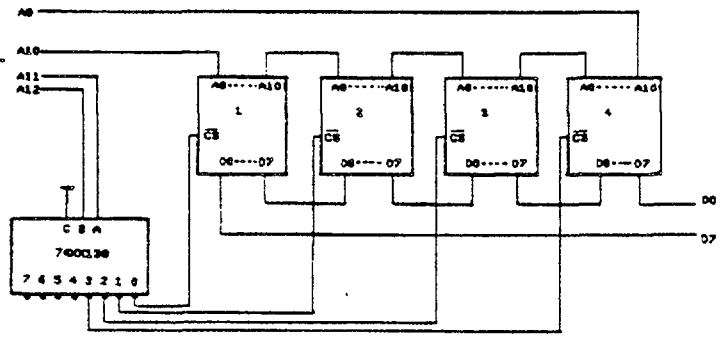


Fig. 3.10.2: Chip selection logic

Most RAM circuits are designed to be connected to a bidirectional data bus structure, like the microprocessors with which they normally work; the same pins are used for input and output. Therefore, associated with each pin there is some kind of transceiver stage. This stage is usually controlled by two lines, labelled $\overline{OE}$ and $\overline{WR}$. If $\overline{OE}$ is HIGH the memory is in the receive mode; data is then stored by applying a negative pulse to the $\overline{WR}$ input (data is latched at the 0 1 edge of this pulse). If $\overline{OE}$ is LOW, memory data is forced onto the bus (read operation). The lines $\overline{OE}$ and $\overline{WR}$ are not supposed to be simultaneously LOW; and, of course, they are only effective while $\overline{CS} = 0$.

Both dynamic and static memories are volatile, that is, their contents is lost at power off. One can create a design such that the memory part of the system, or a portion thereof, is battery backed. The new CMOS RAMs have an extremely low power consumption in the stand-by mode and are very suitable to this application. Some memory circuits sporting a protection circuit with integrated battery are commercially available.

The so-called read only memories (ROMs) are non-volatile devices used in digital systems to store fixed data. The information has been stored on them at some previous time and is permanently available for reading. They are accessed in the same way as RAMs. Their contents can either not be modified at all, or can be rewritten only after erasure by some pnysical process. The following ROM types can be distinguished:

- Mask ROMs: information is coded on them by the last metalization mask on the chip fabrication process; contents can not be modified; economics forbids the production of such ROMs in small quantities.
- Fusible-link PROMs: user programmable by blowing selected internal fuses with a PROM programmer; contents can not be modified; implemented in fast TTL circuits.
- EPROMs: user programmable; can be rewritten after erasure of contents by adequate exposure to UV light.
- EEPROMS: similar to EPROMS but electrically erasable; they can be rewritten within the system after an erasure pulse has been applied; the write operation takes, however, a few milliseconds.

Assemble the circuit shown in the schematic diagram of Fig.3.10.3 on a ready-made printed board.

EXPERIMENT

1. Connect jumper J1 to V_{CC}. With switch SW in the WRITE position, select an address with the switches SWA1-SWA8 and SWB1-SBW4. Be sure that the SWB5-SWB8 are closed and explain why this should be so. Take a note of the selected address in hexadecimal or binary forms. Choose an input data value with SWC1-SWC8 and take a note of this value. Press pushbutton PB to write the data in the selected memory location (pushbutton PB when pushed resets the RS flip-flop [pin 8 LOW]; when released, sets the flip-flop). Repeat this procedure a few times with different values for address and data.

2. With switch SW in the READ position, select again the first address you have written. Push PB and verify if the bit pattern that appears on the 8 LEDs that are connected to the 74XX573 latch is what you expect. Check the other memory locations in the same way.

3. Change jumper J1 to the $\overline{WR}$ line and make a read and a write operation. Compare this situation with the previous one and explain why data is now latched both when writing to memory and reading from it.

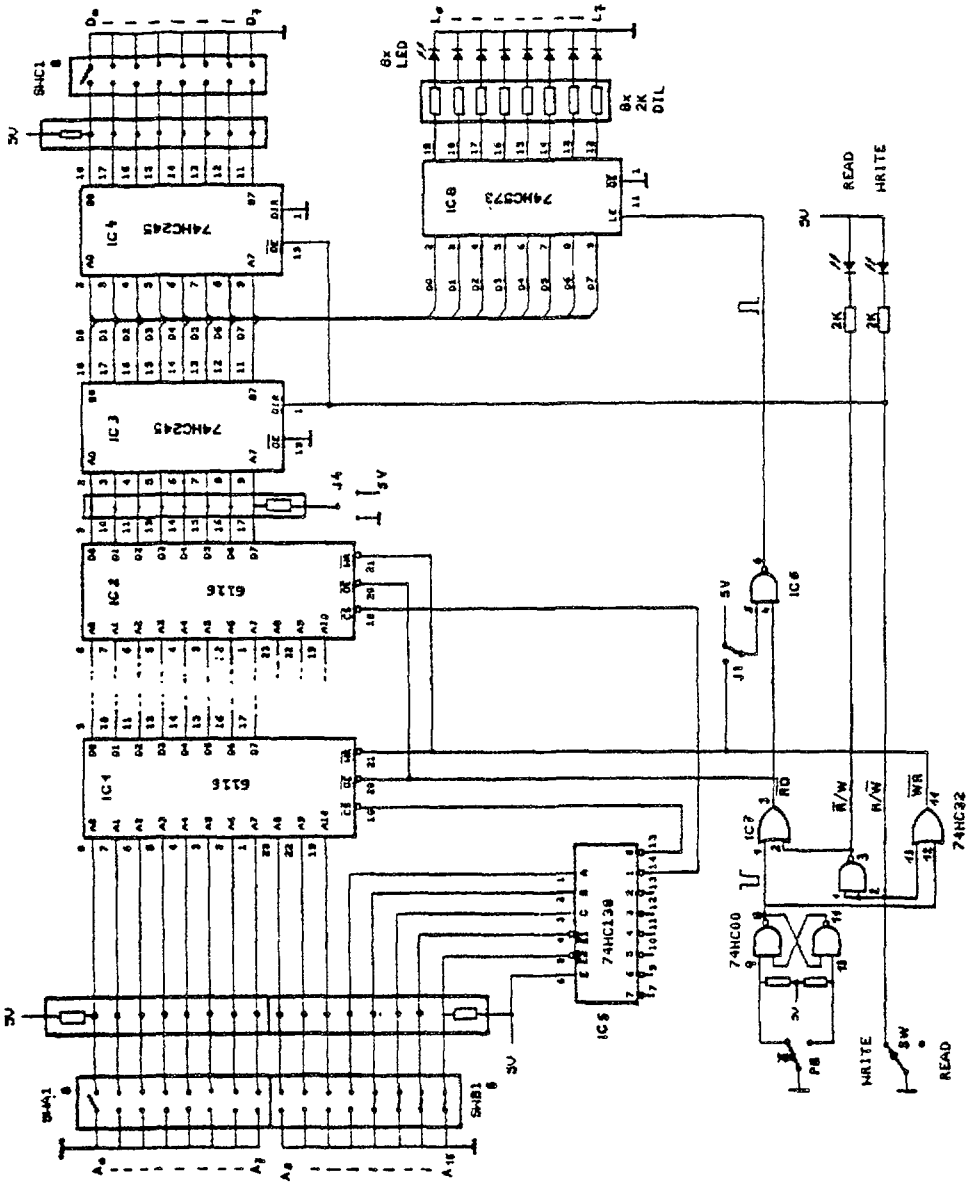
4. With SW in the WRITE position, push button PB and keep it pushed [pin 8 kept LOW]. Modify some of the data bits with SWC. Note that the information displayed by the LEDs is being simultaneously modified. Release PB to store the data both in memory and in the latch.

5. With switch SW in the READ position, push button PB and keep it pushed. Select different memory addresses and read their contents from the LEDs. Check if what happens when no memory chip is selected (use one enable input of the 138 to do this) is what you expect. Discuss if you may expect different things to happen when you use TTL or CMOS circuits for the 245 transceivers. Connect the resistor network RN5 to V_{CC} to use pull-up resistors or to ground to use pull-down resistors. Explain why one or the other of these connections helps to increase the reliability of the circuit.

6. Replace the 373 latch by a 374 flip-flop. Following these replacement, discuss if there are any changes in the schematic diagram that you would like to recommend.

Fig. 3.10.3:

Shematic for memory experiment.



EXPERIMENT 3.11

SYSTEMATIC DESIGN OF SEQUENTIAL CIRCUITS

OBJECTIVE

The objective of this experiment is to present a simple and reliable method for the design of synchronous sequential circuits.

REVIEW

A sequential circuit contains both memory elements and combinational components. It may have two or more states. Each one of these states is defined as a specific set of states of all the individual memory elements. For example, to design a system with 4 states one needs 2 memory elements; the states of these 2 elements combine in 2 ^ 2 different ways, each one identifying one state of the system. (Sometimes one may wish to use more memory elements than the minimum required by the number N of desired system states; this may help in some applications to simplify state decoding.)In the systematic design of sequential circuits, D and JK flip-flops are the most commonly used memory elements. In what follows we discuss the design of synchronous systems, which are, in general, to be preferred to asynchronous systems; they are also easier to design than reliable asynchronous systems.

The design necessarily begins with a clear description of the function of the required system. This is generally done by reducing a word description of the circuit behavior to a so-called state diagram. The states are clearly identified in the diagram, as well as the conditions under which state transitions will occur. In synchronous systems the transitions take place at the clock pulse edge. This implies that the conditions for the next transition are fulfilled immediately after the clock edge, but, of course, they are only acted upon at the next clock edge (as discussed in Experiment 3.7).

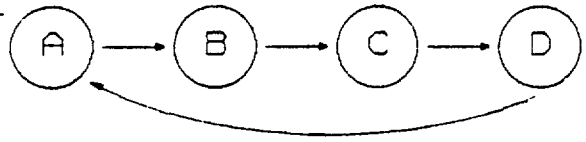
Design example: modulo-4 counters

EXPERIMENT

Let us illustrate the above steps through a simple example, a modulo-4 up counter. Such a counter has 4 states that we arbitrarily label A, B, C and D. Each one of these states corresponds to one of the 4 possible contents of a modulo-4 counter (0, 1, 2 or 3). The state diagram is shown in Fig. 3.11.1. The states are represented by circles and identified by their labels. In this simple example there are no conditional transitions. Transitions take place in the indicated order for every clock pulse. At this stage we may identify each state with a given contents of the counter, say, A → 0 , B → 1 , C → 2 , D → 3 (it could also be D → 0 , A → 1 , etc. or any other combination compatible with up-counting). Next comes an essential step in systematic design: state assignment. To each state A, B, C and D we assign a defined combination of the states Q_1 and Q_0 of the two flip-flops. In principle, this is totally arbitrary; it can be done in any way. But, if, for example, we would like to

Fig. 3.11.1:

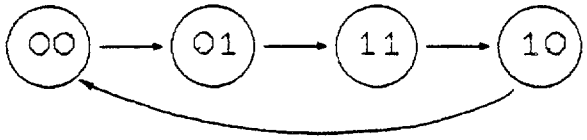
State diagram of modulo-4 counter.



take Q_1 and Q_0 as the outputs of our system; and, further, we would like the outputs to change only one bit when the system moves from one state to the next one, then we would make the following assignment: A → 00 , B → 01 , C → 11 , D → 10. This is the assignment shown in Fig. 3.11.2. Our next step is to write a state transition table with the information available in the state diagram. This table is also shown in Fig. 3.11.2; PS stands for present state, NS for next state.

Fig. 3.11.2:

State diagram and transition table of modulo-4 Grey counter.



PS		NS	
Q_1	Q_0	Q_1	Q_0
0	0	0	1
0	1	1	1
1	1	1	0
1	0	0	0

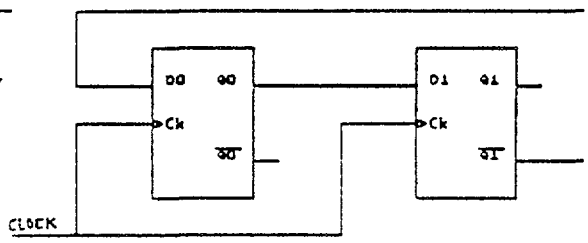
We must now take another decision: which type of flip-flop to use. Again, this is an arbitrary decision; we decide on D-type flip-flops. From the transition table we may now write the equations for the D inputs of the flip-flops, D_1 and D_0D, in terms of the present state values of the outputs. We have

$$D_1 = \overline{Q}_1 Q_0 + Q_1 Q_0 = Q_0$$
$$D_0 = \overline{Q}_1 \overline{Q}_0 + \overline{Q}_1 Q_0 = \overline{Q}_1$$

This is a very simple result, schematically represented in Fig. 3.11.3. Note again that this is a synchronous system. In the present example, the circuit counts the clock pulses in a Grey code (a code where only one bit changes from one number to the next). Check this using the two flip-flops of the 74 package, and make a timing diagram of the circuit operation.

Fig. 3.11.3:

Circuit of modulo-4 Grey counter.



In this simple example, combinational circuits were not required. But suppose that we wanted our state machine (this is an alternate designation for the sequential circuit) to provide decoded outputs, that is, 4 output lines. In each machine state one of the lines would be active (say, 3 lines LOW and one HIGH). Then, of course, a combinational circuit must be used.

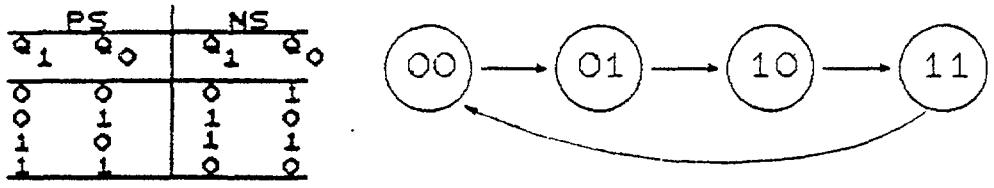
In general, however, combinational circuits have a more fundamental role to play: that of establishing the conditions for the state transitions. We use again a modulo-4 counter example; but now we make the state assignment of Fig. 3.11.4, where the corresponding transition table is also shown. We again choose D-type flip-flops. The equations for the D inputs are

$$D_1 = \overline{Q}_1 Q_0 + Q_1 \overline{Q}_0$$

$$D_0 = \overline{Q}_1 \overline{Q}_0 + Q_1 \overline{Q}_0 = \overline{Q}_0$$

You may verify the design using the two flip-flops of the 74 package. Compare the design to the logic diagram of some of the available integrated synchronous counters.

Fig. 3.11.4:



State diagram and transition table of modulo-4 binary counter.

Let us obtain another circuit with this same function by using JK flip-flops. Instead of two equations, as for the D flip-flops, we now have four equations. Hopefully, this increased writing effort will be compensated by simpler combinational circuitry, made possible by the greater versatility of the JK flip-flop. To derive the equations for the J inputs, we look for 0 1 transitions because J should then be 1. Likewise, for the K inputs we look for 1 0 transitions. We obtain

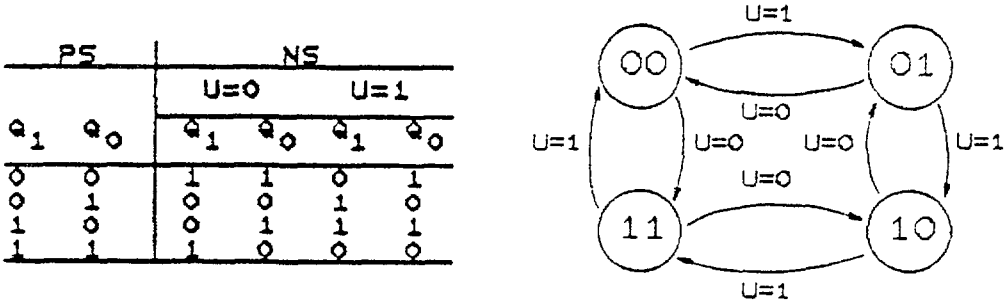
$$J_1 = \overline{Q}_1 Q_0$$
$$K_1 = Q_1 Q_0$$
$$J_0 = \overline{Q}_1 \overline{Q}_0 + Q_1 \overline{Q}_0 = \overline{Q}_0$$
$$K_0 = \overline{Q}_1 Q_0 + Q_1 Q_0 = Q_0$$

Although this is a very simple system, it already shows that using the more versatile JK flip-flop may bring some advantages. Of course, this will depend on the particular design considered. It is clear,for example, that nothing is gained by having JK instead of D flip-flops in a simple shift register.

Design example: up/down counter

Generally, sequential circuits depend not only on the present values of the state variables, but also on the values of input variables. As a design example we take a modulo-4 up/down counter. Count up takes place when the input variable U is HIGH; count down, when U is LOW. The state diagram is shown in Fig.3.11.5 together with the state assignment and transition tables. Let us once again use D flip-flops to implement the system.

Fig. 3.11.5:

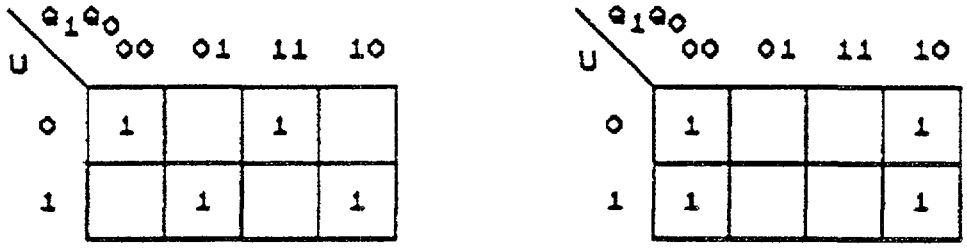


State diagram and transition table of modulo-4 up/down counter.

To find the equations more easily (and in a less error-prone way) we build Karnaugh maps from the state transition table (a brief review of K-maps is given on the end of this experiment). The maps are shown in Fig. 3.11.6. Each box is associated with a defined present state. We put a 1 in the box when the next state to the state associated with the box is a 1 (remember that we are using D flip-flops); it is not necessary to write in the 0's.

Fig. 3.11.6:

K-maps for the up/down counter.



The corresponding equations are

$$D_1 = \overline{U}\,\overline{Q_1}\,\overline{Q_0} + \overline{U}\,Q_1\,Q_0 + U\,\overline{Q_1}\,Q_0 + U\,Q_1\,\overline{Q_0}$$
$$D_0 = \overline{Q_0}$$

You may wish to draw the schematic diagram of the counter and compare it to the diagram of a IC with the same function.

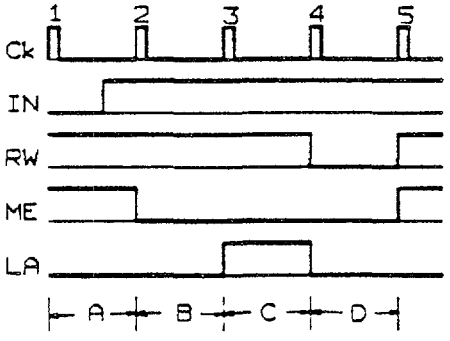
Design example: a controller with 4 states

The previous design examples were chosen to illustrate the design method with simple, well known circuits. Of course, counters are available in many versions and there is little need to design this type of circuits. We now give a design example related to one of the Special Projects discussed later in this Manual.

We wish to design a circuit to control memory operations. The circuit should generate a signal to select read or write operations, a signal to enable the memory IC tri-state outputs, and a further signal to latch the data read from memory into a register. These signals are to be generated according to the time diagram of Fig.3.11.7. Their generation only starts if the value of an input asynchronous variable, labelled IN, is HIGH (IN = 1);otherwise the circuit is idling in a state defined by RW = 1, ME = 1 and LA = 0. Once started, the system completes the sequence indicated in the time diagram independently of the value of the input variable.

Fig. 3.11.7:

Timing diagram of sequencer circuit.



From the timing diagram and the above descriptio n we draw the state diagram of Fig. 3.11.8, where the states are labelled by the letters A to D. In each state we also indicate the corresponding output values in the order RW-ME-LA. The value of the IN variable is also indicated: IN = 1 to proceed from A to B, and IN = 0 to stay in A. For all the other transitions the value of IN may be either 0 or 1 (in other words, IN is a don't care value), and is not explicitly shown in the state diagram.

PS			NS					
			IN=0			IN=1		
1	1	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1	0

(States written in order RW-ME-LA)

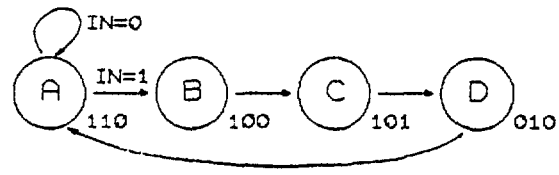


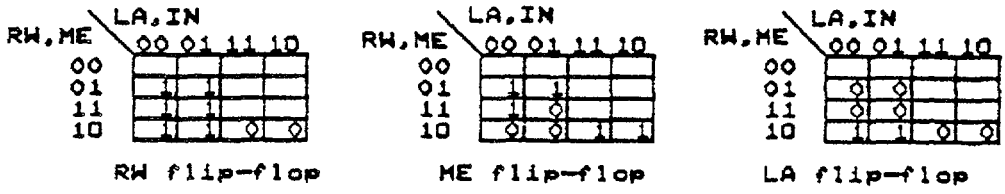
Fig . 3.11.8:

State diagram and transition table of sequancer.

We see that our controller has 4 states. Thus, two flip-flops are required. However, to illustrate what may be done when the system has more states than the ones specified in the its description (this will necessarily happen when $N \neq 2^n$), we decide to use 3 flip-flops. The system will then have 4 unused states. We must make sure that this will not be detrimental to the system, as discussed below. With 3 flip-flops we write the state transition table as shown in Fig.3.11.8. In the table we identify the flip-flop outputs by the labels RW, ME and LA; IN identifies the input variable. From the table we build the K-maps shown in Fig.3.11.9; these are 4X4 maps to include also the input variable.

Fig . 3.11.9:

K-maps for the sequencer.



We now fill in both 0's and 1's; blank boxes belong to the unused states. They are unused but they may occur, either because the flip-flops have no predefined state at power-up, or because an error is introduced into the system by noise. The last event should not, of course, be allowed to happen; but, if it does, we may as well give the system a chance to recover without disconnecting the power supply. Thus we will consider the unused states. All of them should have the idle, 110 state as the next state. Therefore, we fill with 1's the blanks in the K-maps of the RW and ME flip-flops, and with 0's the blanks of the LA flip-flop. We thus arrive at the following equations (the notation RW .D indicated the value at D input of RW flip flop; and similarly for the others)

$$RW.D = \overline{RD} + ME + \overline{LA}$$
$$ME.D = \overline{RD} + ME \cdot \overline{IN} = LA$$
$$LA.D = RD \cdot \overline{ME} \cdot \overline{LA}$$

The system outputs may be taken directly from the outputs of the flip-flops. Our design is now complete and you may wish to test it. You will presumably use two 74 packages and a few gates. (Try a little exercise in boolean algebra if you wish to use only 2 and 3 input NAND gates.) We may, however, implement the circuit in a different way using a registered PAL (see Experiment 3.7). A single PAL16R4 will suffice for the present design, and a number of the PAL inputs and outputs will still be free to implement other logic. The sequencer used in the Special Project referred to above has 8 outputs and is implemented in a PAL20R8 type circuit. Software tools, like the CUPL program referred in Experiment 3.5, apart from being essential to program these devices, offer a great deal of help in the design itself.

The use of Karnaugh maps

Logic functions are described equally well by a truth table, an algebraic expression or a Karnaugh map (K-map for short). A K-map consists of a set of squares where each square is associated with a defined combination of the values of all the function variables. In each square is written the value of the function for that combination of the variables. Seen in this way, a K-map is just a truth table in a different dress; but there is more to it as we will see shortly. In Fig. 3.11.10 we show the truth table, K-map and Boolean expression for a 2 variable function. It is clear that each line in the truth table corresponds to a square in the K-map; the "coordinates" of which are the values of the variables for that line. We did not write explicitly the 0's on the map; where a square is left blank, a 0 is assumed. We could just as well write the 0's and assume 1's in the blanks. Generally, writing 1's is related to expressing the function in minterms, and writing 0's, to maxterms; these names will be defined shortly.

Fig. 3.11.10:

Truth table K-map and Boolean representations.

Let us explicitly define the rules to translate from one representation of the function into another. From the truth table to a Boolean expression we can follow either one of the following two rules:

i) Write the function as a sum-of-products. The products correspond to the lines where the function takes the value 1, and are formed by the variables if they are 1, or by their complements if they are 0. Thus, for the above function, we write $f = \bar{A}\,B + A\,\bar{B}$. (The product on the left corresponds to the second line of the truth table.)

ii) Write the function as a product-of-sums. The sums correspond to the lines where the function takes the value 0, and are formed by the variables if they are 0, or by their complements if they are 1. Thus, for the above function, we write $f = (A+B)\,(\bar{A} + \bar{B})$. (The sum on the left corresponds to the top line of the truth table.)

Similarly, if we start from the K-map. To write the function as a sum-of-products, we look for the squares with 1's. To write the function as a product-of-sums, we look for the squares with 0's.

Each term in a sum-of-products is called a minterm; and each term in a product-of-sums is called a maxterm. The names are suggested by the fact that a function equal to a single minterm fills the minimum possible area of a K-map with 1's, that is, a single square; and that a function equal to a single maxterm fills the maximum possible area with 1's.

Let as see how simplification of a Boolean expression can be obtained through K-maps. Consider the function defined in Fig. 3.11.11. The K-map with 1's is used to obtain the function expressed by its minterms. If it is possible to simplify the expression, we may use for the simplification the rules of Boolean algebra, or proceed directly from a visual inspection of the K-map. It is for this reason that K-maps are useful. In algebra, when we

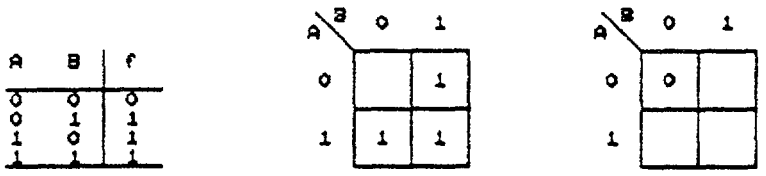


Fig. 3.11.11: K-maps related to minterm and maxterm expansions.

have $X + \overline{X}$ we use the rule $X + \overline{X} = 1$ to eliminate the variable X. This translates into the following K-map rule:adjacent squares with 1's combine to eliminate the variable that is complemented from one square to the other. Thus, in Fig. 3.11.11, the 2 squares with 1's in the left-right direction combine to eliminate B; and those in the top-bottom direction combine to eliminate A. Using this rule, we immediately write $f = A + B$ (this is a function with a single maxterm, as evidenced in the leftmost K-map). We note that the same square can be used more than once in the simplification process. This corresponds to the algebraic rule $A + A = A$.

We now consider functions of 3 variables. The K-map has 8 squares, grouped in a 4x2 lay-out, as shown in Fig. 3.11.12, for a particular function f(A,B,C). In the K-map we can couple the variables in other ways. The essential point is that the paired variables are entered according to a code where only one bit changes at a time (Grey code). This ensures, as in the 2 variable case, that adjacent squares have one variable that is complemented from one square to the other, so that elimination of variables can be made by visual inspection. By adjacent squares we mean squares that are "logically adjacent", not just geometrically adjacent. It is clear that the squares at the extremes of a row (and column) in the K-map are, in this sense, adjacent. Thus, from the above K-map we immediately write $f = A\overline{BC} + \overline{AC}$.

Larger K-maps are built according to similar rules. A 4- variable K-map is shown in Fig. 3.11.13. Again, the essential point is to order the map "coordinates" according to a Grey code so that simplification may be obtained by visual inspection. In the present example of a 4 variable function we can immediately write $f = A + C + \overline{BD}$. The 2 top rows allow us to simultaneously eliminate B, C and D, obtaining the term A. Similarly, the 2 leftmost columns allow us to write the C term. Finally, the 1 on the left bottom square combines with both the top left square and the right bottom square 1's to give the term $\overline{BD}$. This is certainly a fast way to a function in simplified form.

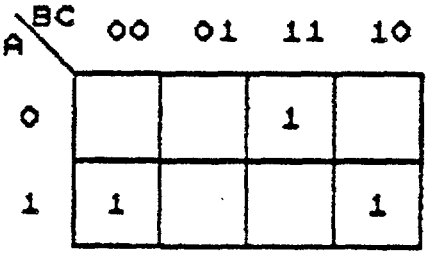


Fig. 3.11.12: K-map for a 3-variable function.

K-maps are frequently used in sequential design when one is determining the equations for the flip flops inputs. In this application, the state variables form the coordinates of the appropriate K-maps and we enter the 1's (or the 0's if we prefer) as required by the state transition table. Each square is associated with a given *present* state; the 1's or 0's show the value required at the inputs of the flip flops to proceed to the appropriate *next* state at the next clock transition.

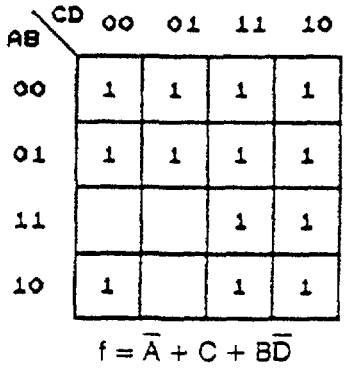


Fig. 3.11.13: K-map for a 4-variable function.

Notes:

EXPERIMENT 3.12

LOGIC ANALYZERS

In this experiment we will learn how to operate a logic analyzer,and will discuss its main functions and controls.

OBJECTIVES

Logic analyzers are important tools in digital circuit development and maintenance. Their input circuitry interprets the input signals in a binary manner as either 0 or 1; the dividing voltage level between these two states may be adjusted for the different logic families, but analog signals are neither measured nor displayed. A large number of inputs, typically 16 or more, may be processed and stored in memory simultaneously. Input data is sampled asynchronously at a rate determined by an internal clock, or synchronously at a rate determined by the clock of the system under measurement.

REVIEW

Logic analyzers are available as stand-alone instruments or as plug-in cards for personal computers. The latter ones are relatively inexpensive and their data acquisition performance is comparable to that of stand-alone instruments.

Analyzer block diagram

The block diagram of a logic analyzer is shown in Fig. 3.12.1.

The input comparator block represents a set of n + q comparators, where n is the number of input data lines and q is the number of qualifiers. Qualifiers are input lines that may be used for trigger purposes but, unlike data input lines, are not displayed. The function of this block is just to provide signals identifying well defined logic levels to the remaining analyzer circuitry. The threshold voltage for the comparators may be adjusted within wide

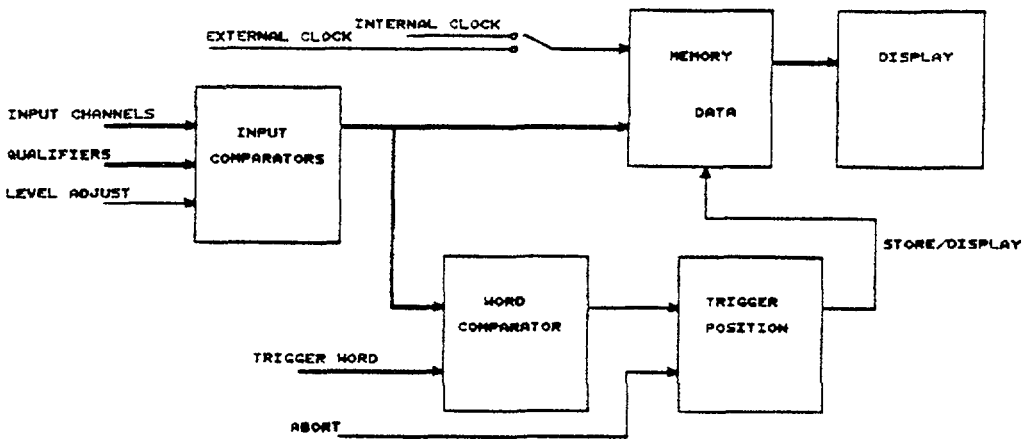


Fig. 3.12.1: Logic analyzer block diagram.

limits in order to comply with the logic levels of the various logic families. Probes are used to take the signals to the comparator. The main requirement on the probes is that they should have high impedance (low capacitance).

The word comparator and the trigger position blocks form the trigger circuitry of the analyzer. The word comparator just compares the incoming word (that is, the set of logical values of the analyzer data lines and qualifiers) to a predefined word (previously loaded in some register). A signal is produced when there is a match between the two words.

The memory is of the shift register type. Each register is associated with one data line, and its length determines the amount of data that can be stored. A register can receive data at its input flip-flop either from the input comparator (acquisition mode), or from its last flip-flop (display mode). In acquisition mode, the clock lines of all registers are activated by the sampling signal; in display mode, by the display oscillator. When external sampling is used, either the rising or the falling edge may be chosen as the active clocking edge. The minimum allowed sample period depends on the particular analyzer; periods as low as 20 ns are common.

The trigger position block controls the memory mode (acquisition or display). It receives its input signal from the word comparator, and sends the memory store/display control signal after a preselected number s of sampling pulses. Thus, s samples are taken after the trigger event is stored. The remaining stored data corresponds to events that occurred prior to the trigger event. An acquisition process may be aborted manually by activating the trigger circuitry directly; this escape action is useful when the expected trigger word fails to appear.

The display shows the stored information either as a timing diagram or as a state table. In the first case, the x-axis represents time in units of the sampling clock period while each data line (usually referred to as a channel) is displayed in a separate band of the y-axis. Data taken at the same sampling time is displayed as a column of points, one point for each channel.

Analyzer operation

EXPERIMENT

The previous description helps one to understand the control commands of a logic analyzer. The following controls are to be expected:

- Sampling clock: internal/external. If internal:select clock rate. If external: select clocking b rising or falling edge;
- Input threshold adjustment;
- Trigger operation: select trigger word and position;
- Acquisition: start or abort;
- Display: timing diagram/state table.

A number of enhancements are provided in most analyzers. For example, choice of code for a state display (binary, hexadecimal or others), use of two memories to allow comparison of two sets of data, or writing data to disk.

A number of simple exercises help one to understand analyzer operation. In particular, the differences between asynchronous and synchronous sampling and, in this case, of rising or falling edge clocking can be understood. Check, for example, the operation of an 8-bit binary ripple counter. Use both internal and synchronous clocks. Try to verify that the counter is asynchronous by detecting intermediate states (as discussed in Experiment 3.8). Observe both state tables and timing diagrams. As another exercise, try to detect the pattern repetition that occurs in the 4-bit pseudo-random generator discussed in Experiment 3.8.

The LSI counter of Experiment 3.9 is also a good training ground. Observe, for example, the 7 segment signals pertaining to a given digit. Here the input comparator level must be adjusted to non-standard values.

Notes:

PART FOUR

MULTICHANNEL ANALYZERS

MCA - an introduction.

Fast growth of the computer technology and its implementation in instrumentation has strong influence on the multichannel analyser. Until several years ago, we only knew the stand-alone MCAs. Now, there are a number of attractive alternative available: separate ADCs as NIM modules with some intermediate memory, linked to the computer seems to be more economic choice. Also many add-on units, converting personal computer into the MCA can be found on the market.

Wilkinson type converters are still the dominant ones. The conversion clock runs as fast as 450 MHz. However, at the channel number of 16,000 the conversion time can not be shorter than 30 μs. Therefore new techniques, like successive approximation conversion and flash conversion not used before in MCA, are explored. In these two methods, the successive conversion suffers from the differential nonlinearity at least ten times bigger than in the Wilkinson type converters. This deficiency is compensated by using sliding scale correction. Tomorrow technology will bring the additional improvement.

Therefore, few converting techniques are studied in Part Four. Results are used in the design of the Wilkinson converter which can communicate with the host computer through the Computer ADC link. The last two topics are placed to the Part Six of this Manual, due to their complexity.

EXPERIMENT 4.1

PULSE STRETCHER

To study properties of the pulse stretcher, a device for storing the nuclear pulse peak value until the ADC makes the conversion.

OBJECTIVES

Analog to digital converters used in nuclear spectroscopy need a certain time interval to convert the measured voltage into its binary equivalent. Therefore the peak value of pulses from spectroscopic amplifiers must be kept until the conversion is completed. This is the purpose of the PULSE STRETCHER shown in Fig. 4.1.1 as a black box.

REVIEW

The requirements on the pulse stretcher are several. It must

1. Detect and hold the peak of a pulse.
2. Tell the ADC that the peak has arrived.
3. Disconnect itself from the source of pulse.
4. Receive a signal from the ADC indicating that the conversion is done.
5. Discharge the peak holding capacitor.
6. Reconnect itself to the pulse source to repeat the process.

Figure 4.1.1 is a block diagram of a circuit which will accomplish these six tasks. The diagram also contains graphs of the waveforms at critical points in the circuit. These and other waveforms also appear in Fig. 4.1.3 in a timing diagram of the pulse stretcher action.

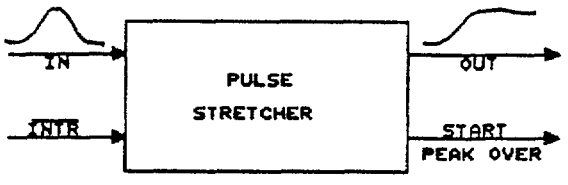


Fig. 4.1.1: Pulse strecher as a black box.

The various blocks of Fig. 4.1.2 will now be discussed in more detail. The discussion will be based on the six tasks listed above.

The first task is the critical task and is performed by the peak height detector. The capacitor is the charge storage device across which the peak voltage appears. The

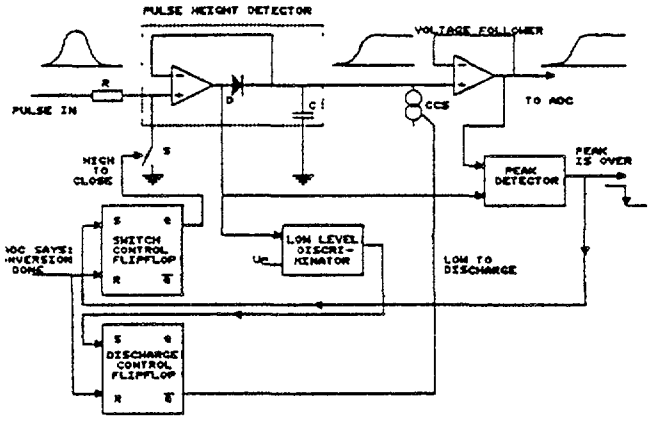


Fig. 4.1.2:

Block diagram of pulse strecher.

operational amplifier and diode is a modified voltage follower which permits the voltage across the capacitor to follow the voltage of the incoming pulse as long as it is increasing, but which prevents the capacitor voltage from going down as the pulse voltage decreases. Clearly as the pulse comes in the + input of the operational amplifier (S is open), the circuit acts as a voltage follower providing current through the diode to C to bring its voltage up to that of the pulse. However, when the voltage of the pulse decreases, the diode prevents current from C discharging into the operational amplifier. Under these conditions the + imput becomes lower than the - input, the operational amplifier acts as a comparator, and its input voltage falls to the negative power supply voltage.

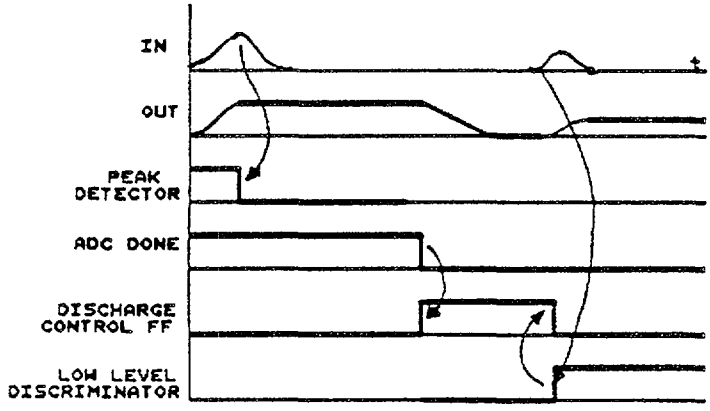


Fig. 4.1.3:

Waveforms.

The diode, of course, keeps the capacitor from discharging, so its voltage remains at the peak voltage of the pulse. The voltage follower is just a device placed in the circuit to prevent the ADC and peak detector from loading the capacitor.

The peak detector is the key to the next two tasks. When the input from the voltage follower, which is equal to the voltage across the capacitor (the pulse peak), is greater than the output of the first operational amplifier (which goes very low when the peak is passed) the output from the peak detector falls. This fall signals the arrival of the peak, tells the ADC to start the peak measurement, and tells the switch control flipflop to close S1, thus isolating the pulse detector from the source of the pulses by grounding the + imput of the first operational amplifier.

The control flipflops both receive a signal from the ADC when that device has completed its work thus performing the fouth task mentioned above.

The discharge control filpflop turns on the constant current source which discharges the capacitor completing the fifth task.

The switch control flipflop now opens switch S thus completing the sixth task and making the pulse stretcher ready to receive the next pulse. When this pulse comes in, the low level discriminator detects its arrival and turns off, through the discharge control flipflop, the constant current source capacitor discharge circuit.

Those with a good understanding of nuclear electronics will immediately recognize a few difficulties with this circuit. There is a small timing problem. At the instant S was opened so that pulses could again be received, the capacitor had not yet been fully discharged. Thus the circuit was not really ready to receive more pulses. However no damage can be done; because, if the pulse is too small, it will be ignored by the peak detector and, if it is large enough, it will be measured correctly. The net effect is just a small increase in dead time. It would not take a very complicated digital circuit to solve this problem. Also the input operational amplifier saturates in the negative direction. Any saturated semiconductor requires a relatively long recover time. The diode in the pulse height detector has a finite reverse current which will tend to discharge C. The switch and several other blocks have yet to be detailed. Try your hand at sketching a working circuit for these blocks.

A working version of this pulse stretcher including a few improvements is given in Fig. 4.1.4. First carefullly identify all the components in Fig. 4.1.4 with the correct block in Fig. 4.1.3. It is easy to identify Q1 with S, U3 with the peak detector, U4 with the low level discriminator, and the BC182 transistors with the constant current source and its control.

The voltage follower has been incorporated into the feedback loop of the first operational amplifier and a diode added to compensate for the finite reverse resistance of the diodes. The diode D1 has been added to prevent U1 from saturating in the negative diredtion by preventing the output from going below -0.7 V. The resistors, R1 and R2, and capacitor, C1, were added to prevent oscillations. The resistor, R3, is a decoupling resistor.

EXPERIMENT

Assemble the circuit and check its operation. How stable is the stored voltage? The time stability can be improved by introducing a larger valued capacitor, C2. However, now the circuit can not respond properly to very short pulses. Estimate the relation between the pulse width and capacitance for the value which will allow the proper pulse height registration.

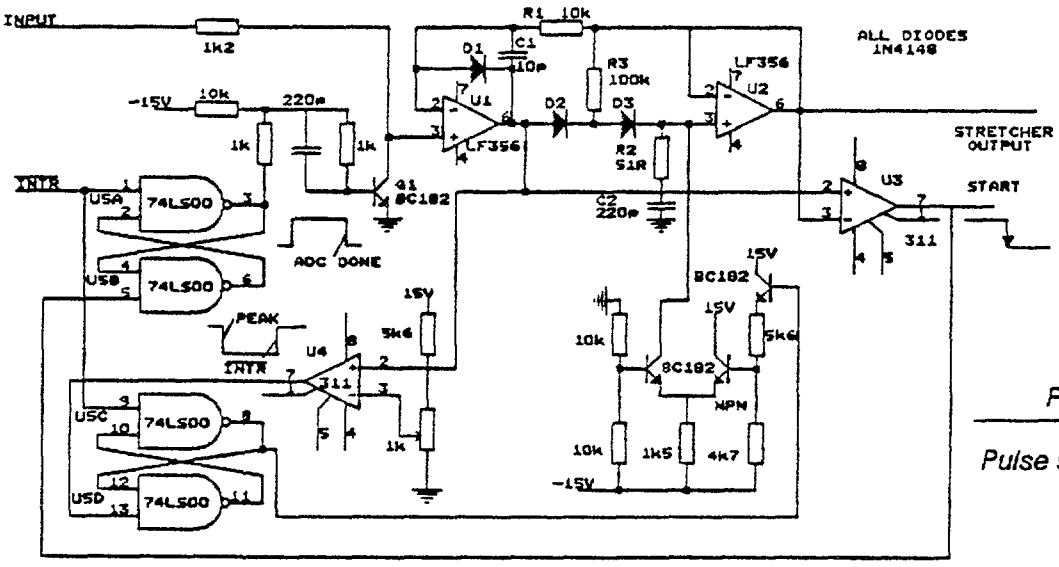


Fig. 4.1.4:

Pulse strecher.

Notes:

EXPERIMENT 4.2

DEMONSTRATION WILKINSON TYPE ADC

OBJECTIVES

A basic Wilkinson type ADC converter is studied. The result leads to the design of the practical version presented in Part Three as a special projects.

REVIEW.

The analog to digital converter (ADC) is the heart of the multichannel analyser. We will study the operation of a simplified version of the Wilkinson type ADC. The task is illustrated by Fig. 4.2.1. The unknown voltage U_x is connected to the input INP. When unit is activated by a pulse at the START input it takes a sample of the input voltage, and provides its binary equivalent at the output. The 8-bit output data D0-D7 are valid after appearance of the EOC (End Of Conversion) pulse.

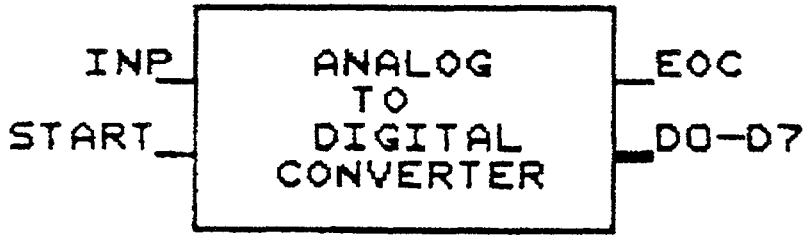


Fig. 4.2.1: Black box representation of the converter.

The block diagram of our ADC is given in Fig.4.2.2.

To perform the conversion, the actions shown in Fig.4.2.3 are taken:

1.Normally transistor Q1 is conducting because of the high voltage at the collector of the transistor Q2. When a positive pulse is applied to the START input the signal from input INP appears at the noninverting input of the operational amplifier U1. The voltage across capacitor C was zero; therefore output voltage of the operational amplifier becomes high. Current flows into C until the voltages at the inverting and noninverting inputs are equal. The START pulse should be long enough to allow full charging.

2. The START pulse inverted in Q2 and INVERTER clears counter.

3. START pulse is over.

3.a. Its descending side reaching ONE SHOT through the Q2 and INVERTER triggers ONE SHOT which produces short pulse.

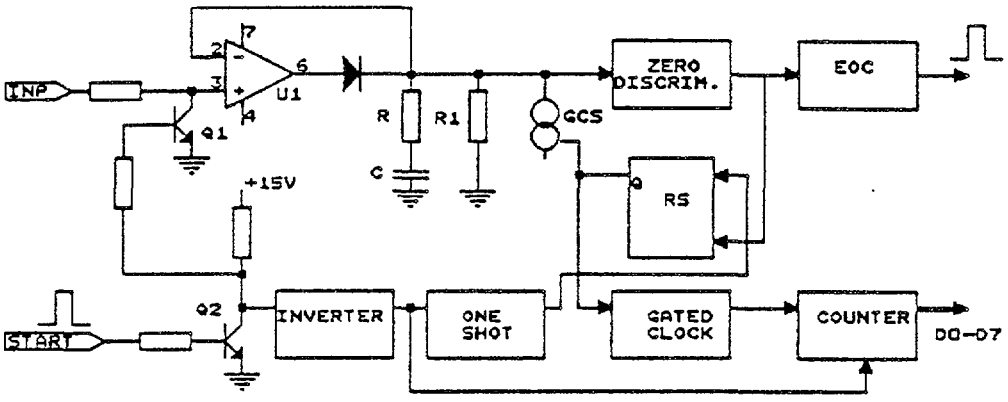


Fig. 4.2.2:

Block diagram of the converter.

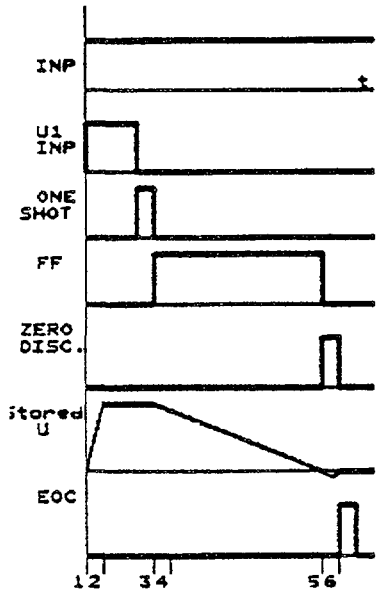


Fig. 4.2.3:

Waveforms.

3.b. The input gate transistor Q1 becomes again conducting. The noninverting input of the operational amplifier is grounded. Because of the positive stored voltage across C, the output of the operational amplifier goes to the negative saturation. The circuit situated left of the diode has no more influence.

4. The pulse from ONE SHOT is over. RS flipflop is set.

4.a. GATED CLOCK starts to provide pulses to COUNTER.

4.b. CONSTANT CURRENT SOURCE is activated. Because of the constant current drawn from the capacitor C the voltage across it descend linearly. The capacitor discharging time will be proportional to the initial voltage across the capacitor.

5. ZERO DISCRIMINATOR announces zero voltage across capacitor.

5.a. The pulse generated at the ZERO DISCRIMINATOR output reset RS flipflop. CONSTANT CURRENT SOURCE is disconnected; the voltage across the capacitor emains zero.

5.b GATED CLOCK is stopped. The final number in the COUNTER is proportional to the counting time and thus to the measured voltage.

6.

6.a.At the noninverting input of the operational amplifier is a small positive voltage from Q1. The voltage at the inverting input (equal to the voltage across the discharged capacitor) is zero. Therefore the operational amplifier output voltage will go high, and will charge capacitor until the difference between inverting and noninverting input will be zero. The resistor R1 connected in parallel with the capacitor C will draw a continuous small current from the amplifier through the diode into the capacitor. This resistor prevents noise from driving the voltage in the capacitor negative. That is, the amplifier keeps the voltage on C from drifting above zero, abd R1 keeps the voltage from drifting above zero

6.b.ZERO DISCRIMINATOR output will be low; RS flipflop can be activated again if a START pulse will appear

Now we can define the units which are black boxes in the block diagram (see Fig.4.2.4).

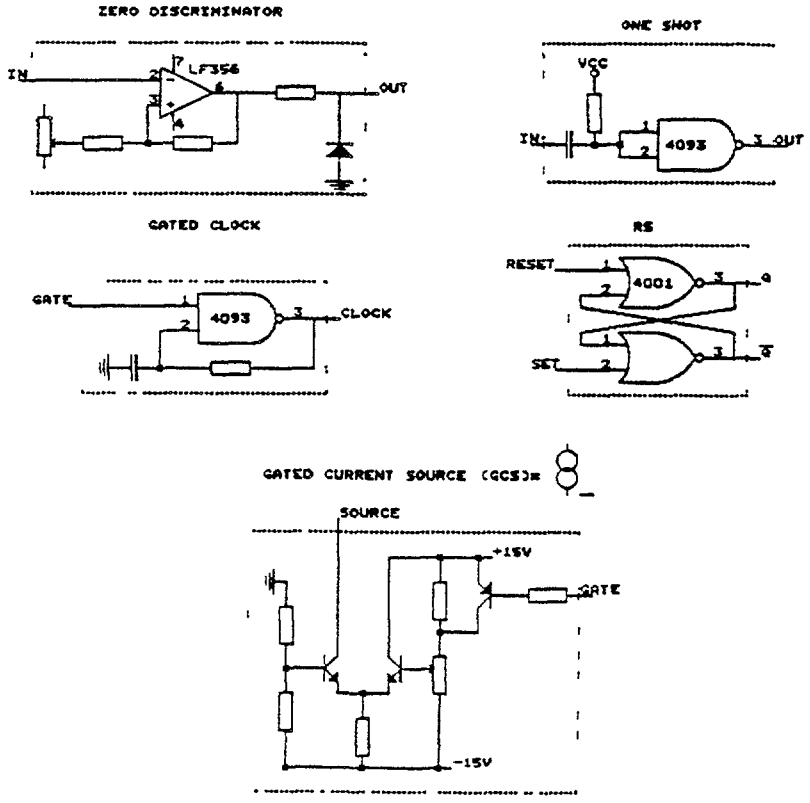


Fig. 4.2.4:

Basic units of the converter.

The ZERO DISCRIMINATOR should have small input current. We can use the LF356, op amp with FET inputs. Some positive feedback will improve the response. Its output swings between both the supply voltages. It must be limited in the negative direction to accomodate the CMOS circuits we intend to use in the EOC and RS flipflop.

EOC unit is one shot, triggered by the falling edge side of the ZERO DISCRIMINATOR output. The CMOS circuit 4093 (a quad NAND gate with hysteresis) makes a simple one shot.

ONE SHOT should be triggered by the HIGH to LOW transition. Circuit is identical with the EOC block.

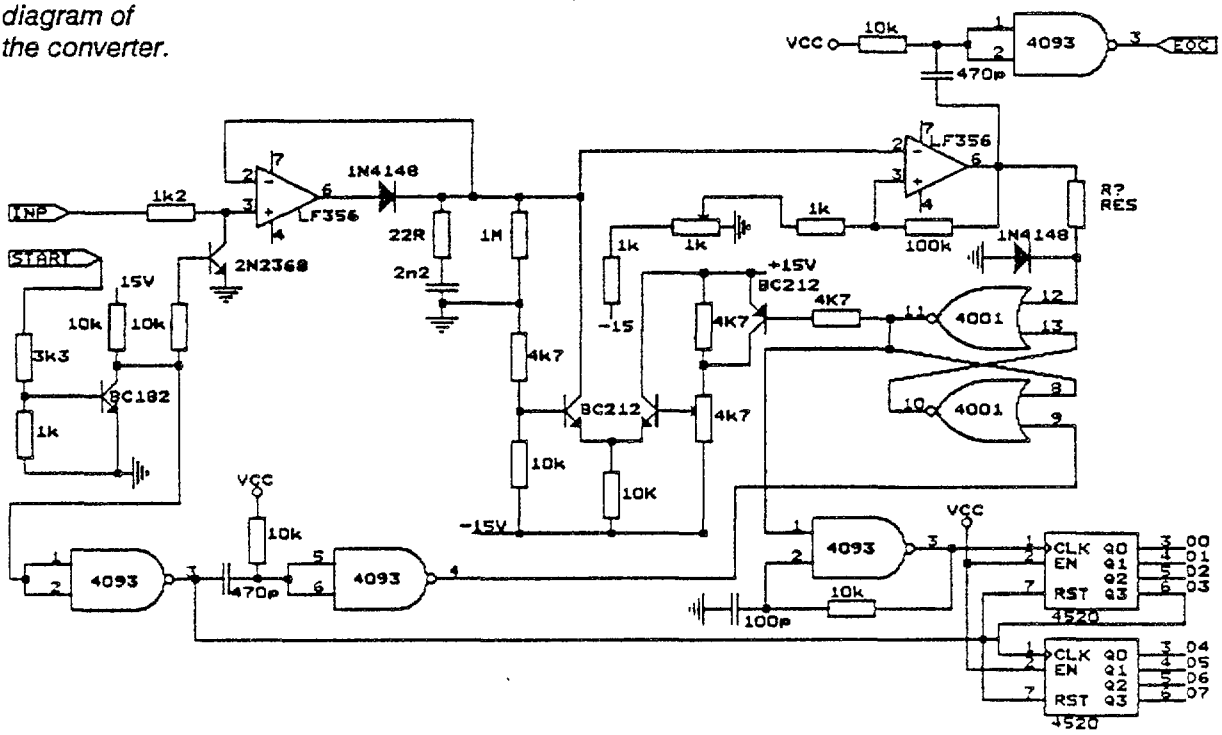
GATED CLOCK is a relaxation oscillator made with a 4093. It oscillates when the gate is HIGH.

RS flipflop is made of two NOR gates from a 4001.

The GATED constant current source (GCS) was studied in one of the previous exercises. In Fig.4.2.4 is shown the modified version using a CMOS signal for gating.

Fig. 4.2.5: The detailed wiring diagram is given in Fig.4.2.5.

Wiring diagram of the converter.



EXPERIMENT Assemble the circuit and try to develop a checking procedure. Apply positive constant voltage of a few volts to the input INP and periodic (lkHz) TTL pulses of the 10 μs duration to the START input.

Verify the operation and make critical remarks. Give suggestions as what should be improved to achieve professional performance.

Is the new circuit good enough so that a few additional bits can be implemented? The answer can be obtained by studying the channel profile.

Connect an input voltage corresponding to the full range.Increase the voltage very slowly and observe the last bit on an oscilloscope. It will be low within the definite voltage range, then high, then low again. In the case of an ideal ADC these transition should occur at a precisely defined voltage as shown in Fig. 4.2.6. However, in our case, there will be a smooth transition from low to high and later from high to low.

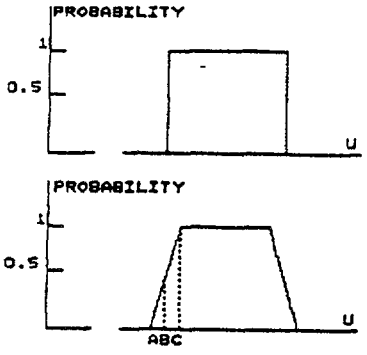


Fig. 4.2.6: Determination of the channel profile.

It is possible to find the input voltage at which the last bit is still low all the time (A in the lower part of Fig. 4.2.6). Then we can find the voltage at which the last bit is half of the time low (in random sequences), and half of the time high (B in the same figure), and finally the voltage when it is high all the time (C). After repeating the same procedure at the opposite side we have the channel profile. Sharper are transitions between two subsequent binary readings, more higher bits can be introduced.

Notes:

EXPERIMENT 4.3

SUCCESSIVE APPROXIMATION ADC

OBJECTIVES

This experiment introduces some of the basic concepts of direct analog to digital conversion through the construction and analysis of a very simple circuit.

REVIEW

There are a number of differences between digital and analog signals. Digital signals are easy to store and manipulate. Analog signals are the signals generated by most real world transducers. An analog signal can take on any value between usually well defined limits. Digital signals can take on only a finite number of values (depending upon the number of bits available) between those same limits. Analog to digital converters (ADC) allow one to change a signal from its analog form to a digital representation.

As an example let us consider an analog signal which can take on any value between 0 and 10 volts. Let us convert the analog signal into a three bit digital number. This means that we create 2^3 (or 8) different bins, each labeled with a different binary number. The job of the ADC is to see that the analog signal is put into the appropriate bin. Of course, the number of bins depends on the number of bits (n) in the digital number according to the relation, number of bins equals 2^n.

Our case is illustrated in Fig. 4.3.1.

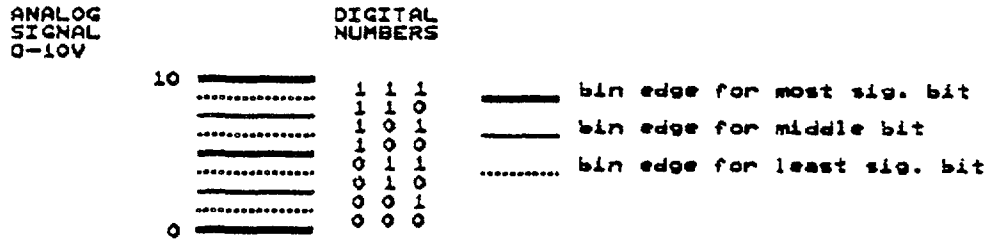


Fig. 4.3.1: Relation between analog signal and digital numbers.

Here the 0 - 10 V range of the analog signal has been divided into eight bins with divisions associated with specific bits. If two bits only were to be used, the dotted lines associated with the least significant bit would be removed leaving only four (2^2) bins. If another bit were available each existing bin would be divided into two giving 16 (2^4) bins. Clearly the more bins the better the resolution, but the more difficult the conversion.

A block diagram for a simple ADC is given in Fig. 4.3.2.

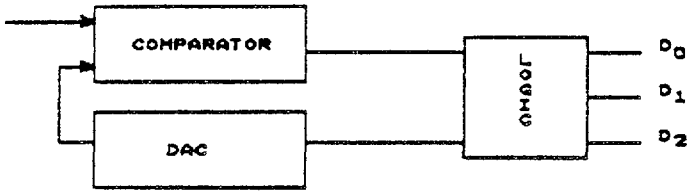


Fig. 4.3.2:

Simple ADC block diagram.

The details of the logic block depends strongly on the type of ADC one has, but in many it takes the output of the comparator and generates a trial digital number. That number is fed to the DAC. Again the DAC can take a number of forms, but all forms output an analog signal proportional to the digital number. That signal is compared with the original signal in the comparator and the result returned to the logic block for further processing. And so the system repeats itself until the correct digital number is found.

Next build up a very simple example of this ADC. A possible comparator circuit is shown in Fig. 4.3.3.

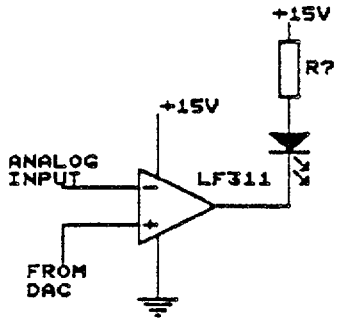


Fig. 4.3.3:

Comparator circuit.

The comparator is a low input current, open collector output comparator. In this case it drives a LED which is to be lit when the input from the DAC is less than the analog input.

The DAC circuit here is a resistor ladder network as shown in Fig.4.3.4.

Other DAC circuits such as the one studied in experiment 2.2 could be used, but this circuit has the advantage of being passive, giving an output of the right polarity, and being used in the next experiment. The DAC is the key block in the circuit. The utility of the ADC depends on the accuracy with which the DAC defines the edges of the bins.

The logic block used here consists mainly of three switches and an EPROM and control logic. See Fig.4.3.5.

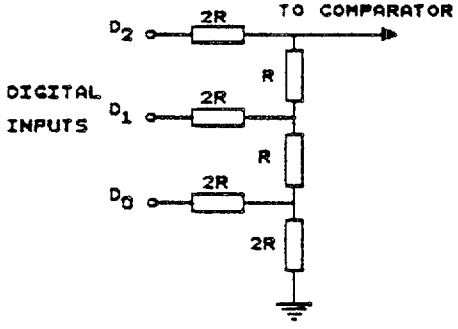


Fig. 4.3.4:

Ladder DAC.

EXPERIMENT

Build the working circuit shown in Fig. 4.3.6.

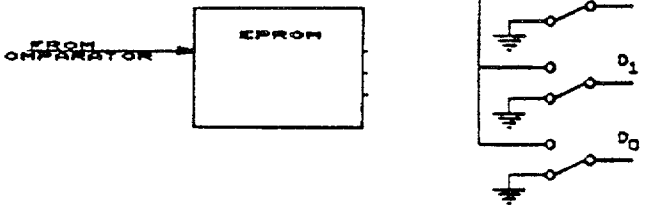


Fig. 4.3.5:

ADC logic block.

You will immediately recognize all the blocks we have discussed and you will see that no details of the EPROM have been given That is because you will be the EPROM. And you will now be programmed.

Start with all the switches grounded, that is in the O or low state. Place a voltage on the input. The green comparator LED will be on indicating that the analog signal is higher than the digital number. Change the state of the most significant bit (msb) switch (D2).

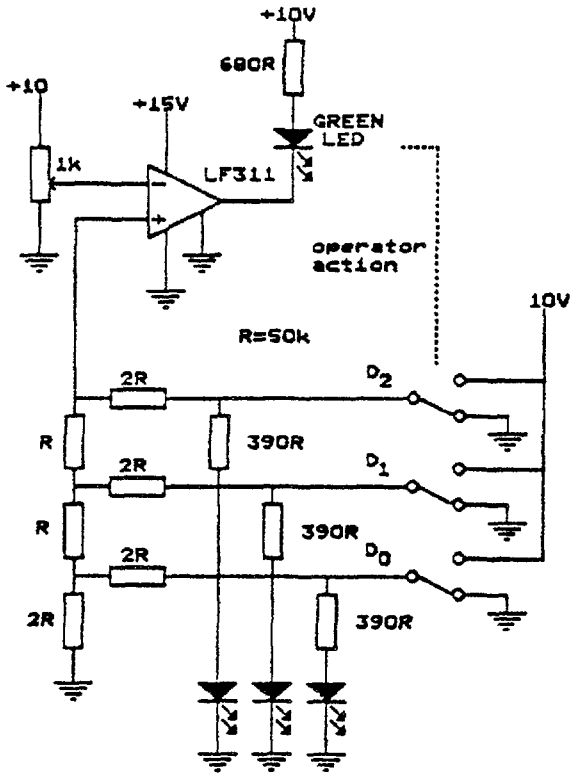


Fig. 4.3.6:

Simple successive approximation ADC circuit..

That action establishes the floor of the appropriate bin at 5 V, half way to the 10 V maximum (See Fig. 4.3.1). Your next action depends on whether the LED remains on or is turned off.

If the green comparator LED is still on, you know that the analog voltage is higher than the digital number; and that the msb is correctly set. Now turn your attention to the second bit. *If, however, the green LED is off, you know that the analog voltage is lower than the* digital number; and that the msb is too high. Turn it off to the correct state and turn you attention to the second bit as before. Repeat until all the bits are set correctly. Note that this procedure provides for the fewest possible switch settings.

Convert a few different analog voltages into digital numbers. Carefully measure each of the bin edges. Are all the bins in exactly the correct place? Are they all exactly the same width? From where do the discrepancies come?

Devise a procedure to make the circuit mimic analog to digital conversion by increasing steps. Compare the number of switch changes in this method with the previous method. Note that the average number of switch changes in this method increases in proportion to the number of bits in the ADC. The increase in the successive approximation ADC is proportional to only the logarithm of the number of bits. Devise a procedure to make this circuit mimic a tracking ADC. Under what circumstances would this new type be better than the original procedure?

In actual practice the logic block would receive a signal to start the conversion procedure, and it would send a signal out when it was done with the conversion. The input would be taken from a circuit like the pulse stretcher studied at the beginning of this chapter. Of course, in practice the switching would be done automatically with logic.

One possible arrangement to do this automatic switching is shown in Fig. 4.3.7. This circuit is actually a complete four bit successive approximation ADC. Locate the sub-sections which you have already studied. The comparator is on the left. The DAC resistors are on

the top. The IC U2 provides the pulses to run the JK flipflops (one for each digit) in the middle which sets its bit and then checks the comparator to see if it should remain set. This part of the circuit automatically does what you did with the switches in the circuit you built. The latch provides the end of conversion (EOC) signal discussed in experiment 4.1. This particular circuit does not have a provision for receiving a START signal. It just runs continuously. A RS flipflop on the clock input would provide for the START signal.

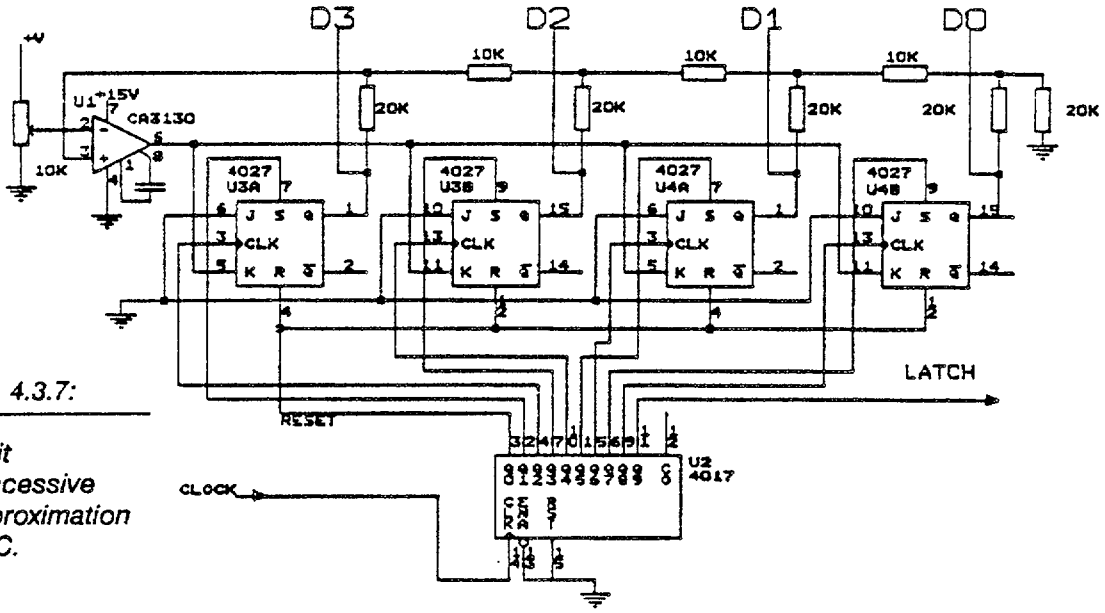


Fig. 4.3.7:

4-bit successive approximation ADC.

EXPERIMENT 4.4

SLIDING SCALE CORRECTION OF SUCCESSIVE APPROXIMATION ADC

OBJECTIVES

The objective of the experiment is to demonstrate the importance of the sliding scale correction in successive approximation ADC's and to present the design principles of one suitable circuit for implementing the correction.

REVIEW

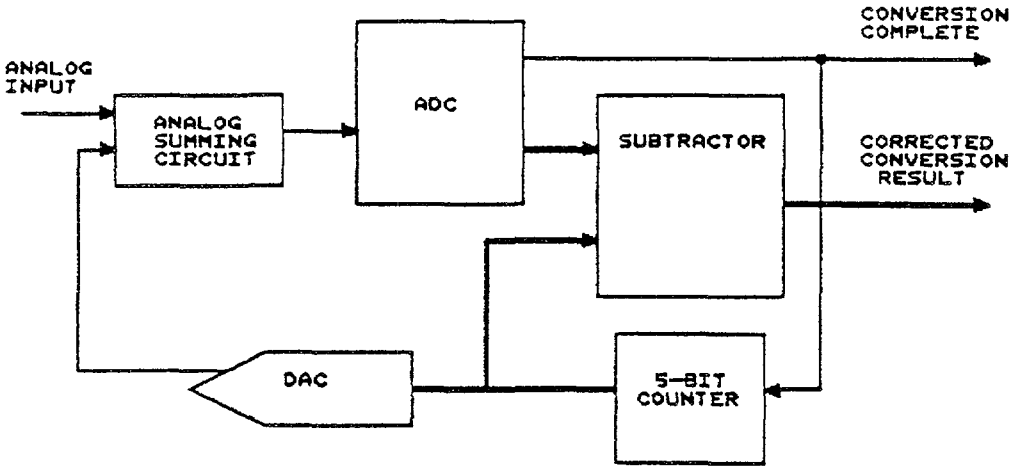
Successive approximation ADC's built in integrated form, are relatively fast, accurate, inexpensive, and easy to use devices. However, in spectroscopic applications an essential requirement is that the channel width be uniform; otherwise the system will show differential linearity. This uniformity is a built-in characteristic of the Wilkinson-type of ADC, where the width of every channel is determined by the same physical elements. In successive approximation (and in flash type) ADC's the channel width for the various channels is determined by different groups of a set of physical elements, such as the group of the more significant ladder-network resistors for a given value of the successive approximation register. The result is that the uniformity of the channel width is sufficiently poor to preclude its use in spectroscopic applications if no suitable correction is made. This problem is discussed in TECDOC 363 and will not be described in detail here. A suitable correction procedure is to add to each input pulse an amplitude correction corresponding to a given multiple of the average channel width, w. To see this, assume that the input pulse amplitude corresponds to channel c and that the added voltage, v, corresponds to n average channels ($v = n \times w$). An ideal ADC would then give a conversion value $c + n$, and the correct result is obtained by subtracting n from this conversion value. If the number n of added channels varies randomly between 0 and N for each new pulse of amplitude c, the effective channel width of the channel associated with these pulses is the average of the widths of all channels from c to $c + N$. Thus the effective non-uniformity of the channel widths is greatly reduced. (Read a detailed discussion in TECDOC 363.)

The sliding correction voltage, $v = n \times w$, is easily obtained from a digital to analog converter (DAC) of precision similar to the ADC, but using only a set of the most significant bits. This voltage, appropriately scaled, is then summed to the incoming pulse and the corresponding value of n is to be digitally subtracted from the conversion result.

The block diagram of a such a correction circuit is shown in Fig.4.4.1.

Fig. 4.4.1:

Block diagram of sliding scale correction circuitry.



Before a brief discussion of the detailed circuitry, a comment should be made. A 5-bit counter, incremented at the end of each conversion, drives the DAC; thus the correction voltage, v_c, follows a definite pattern when proceeding from one conversion to the next. This is of no consequence if one is analyzing pulses from a detector. As discussed in TECDOC 363, it is unsuitable for use with ramp generators or other devices whose output pulse follows a definite pattern (a pseudo-random generator is discussed as an application of shift registers in Experiment 3.8).

A circuit that implements the above block diagram is shown in Fig.4.4.2. It uses a 8-bit ADC (256 channels) and a 5-bit correction voltage (32 channels). Thus the sliding scale corrected ADC has 224 channels.

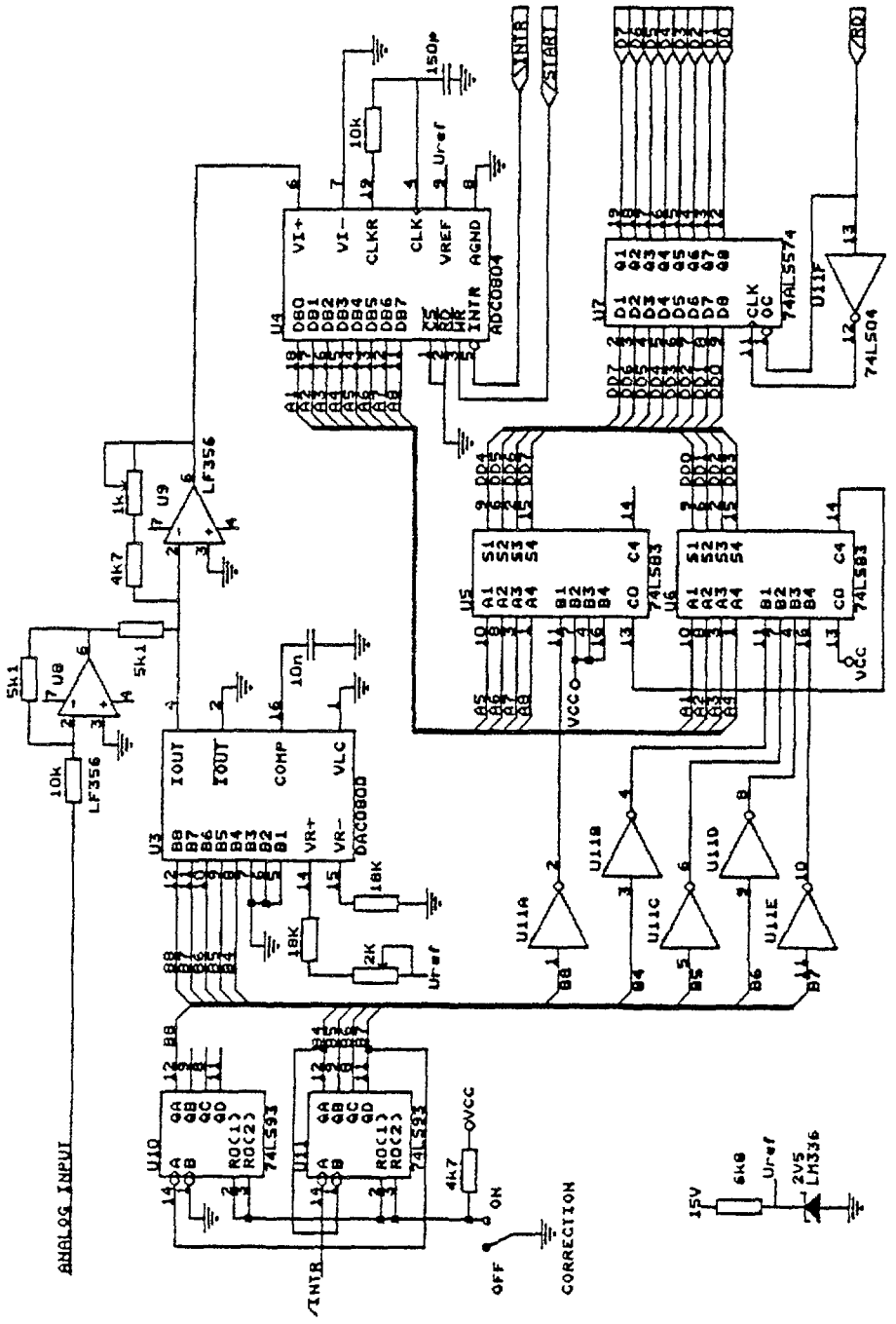
We now make a few comments on the schematic, leaving its detailed interpretation as an exercise. The subtraction is performed in two 83 adders using the two's complement of the number to be subtracted. This complement is obtained by inverting all the bits (one's complement) and then summing 1 to this number (through the carry input of the lowest weight adder). The ADC data output is permanently enabled; the tri-state circuitry required for connection to a bidirectional data bus is provided by the 574 octal flip flop. An $\overline{RD}$ signal is inverted to clock the corrected conversion result into the 574 and the active low RD enables its tri-state output buffer.

EXPERIMENT

You should assemble the prepared circuit board and try it with signals from a NaI detector. The switches shown in the schematic of Fig.4.4.2 will allow you to easily compare the results obtained with an uncorrected successive approximation ADC with those obtained with the sliding scale correction. The results are displayed in the computer to which the circuit is to be connected The connection details are discussed in the ADC computer link project in part 6 of this manual.

Fig. 4.4.2:

Schematic of sliding scale correction circuit.



Notes:

EXPERIMENT 4.5

VOLTAGE TO FREQUENCY CONVERTERS

The objective of this experiment is to present voltage to frequency converters and to discuss the design of current and voltage integrators built around these converters.

OBJECTIVES

The A/D converters used in pulse-height analysis belong to the Wilkinson type or to the successive approximation type coupled with suitable correction circuitry for channel width non-uniformity. Flash type A/D converters are used in experiments where high speed is the main concern and an appreciable degree of differential non-linearity can be tolerated. All these type of converters act on an "instantaneous sample" of the input signal. They are intrinsically non-integrating converters.

REVIEW

In experiments related to nuclear applications there is also a need for A/D converters of the integrating type. Such is, for example, the case for the measurement of the total beam charge in an accelerator experiment. Beam charge is obtained by integrating beam current. With modern ICs, this can be accomplished in an accurate way without too much difficulty. In the present experiment we discuss a circuit designed around the LM331, an integrated voltage-to-frequency converter (VFC) that can attain 0.01% precision (roughly equivalent to 1/2 LSB in a 12 bit ADC).

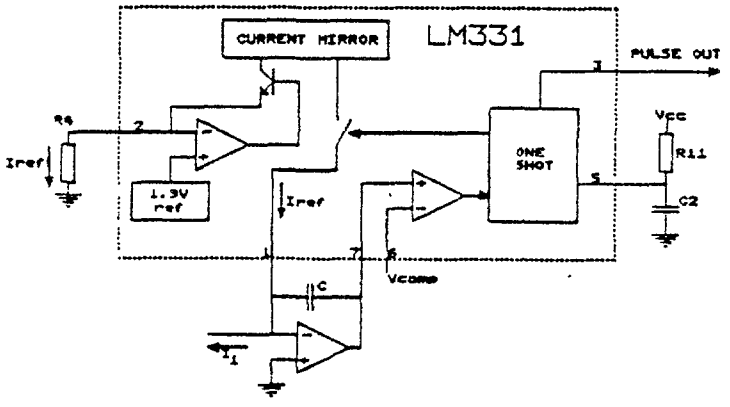


Fig. 4.5.1: VFC operation principle.

In Fig.4.5.1 we present a diagram that illustrates the operating principle of the designed circuit and spotlights the critical components external to the LM331. The input current I_i is integrated in capacitor C through the action of the operational amplifier. The comparator inside the 331 triggers the one-shot which, in turn, closes the switch. A constant current I_{ref} of opposite polarity to I_i is then injected into the integrating capacitor C for a time τ determined by the one-shot. The charge transported by the input current I_i during this

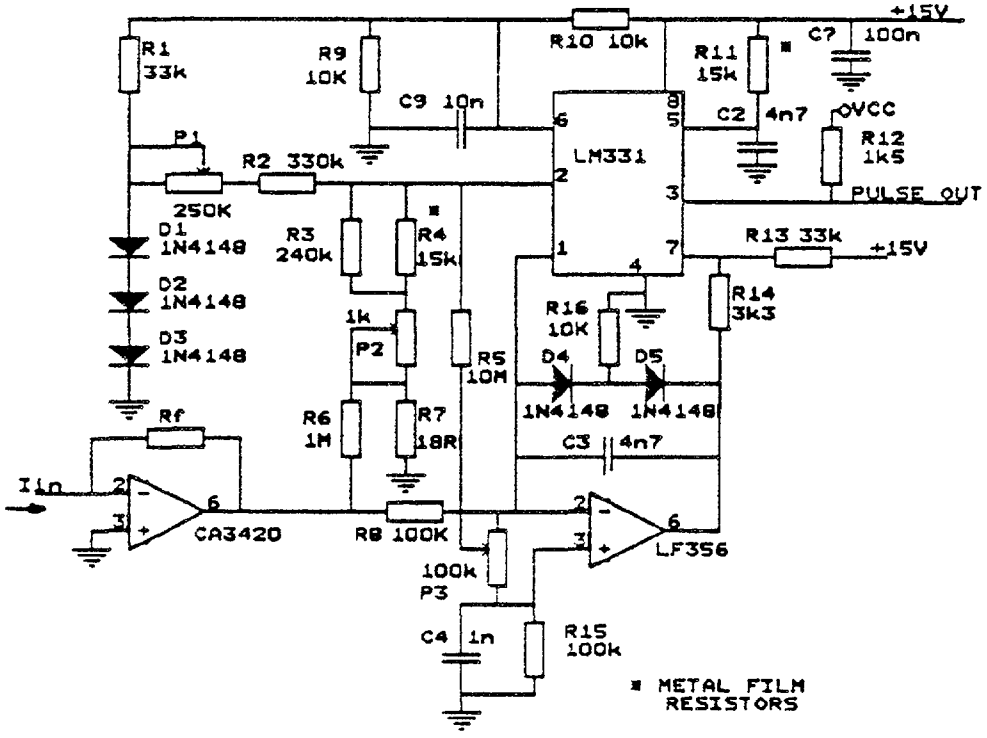
EXPERIMENT

time should be less than $I_{ref} \cdot \tau$ (otherwise the system will not operate, as you may see from this discussion). Therefore, the comparator returns to the initial state and a new cycle begins. An output pulse is produced each time the one-shot triggers. The frequency of these pulses is proportional to the average input current. The total pulse count is proportional to the total charge transported by the input current.

External components critical to the circuit accuracy are labelled in the simplified diagram with the number they have in the detailed circuitry of Fig. 4.5.2. The comparison voltage V_{comp} is not critical; it does not matter the threshold at which the I_{ref} balancing current is switched on. V_{comp} is obtained from the supply voltage through a dividing network. Resistor R4 determines the reference current, I_{ref}; R11 and C2 determine the time τ during which I_{ref} flows to the integrating capacitor. Therefore these components are critical for measurement accuracy. The capacitor should be of polystyrene or other high quality type. The resistors should be metal film and track closely with temperature. In fact, if R11 increases, the time during which I_{ref} is flowing increases; but, if R4 also increases, the balancing current is reduced thereby compensating the time increase). The operational amplifier is, of course, required to have negligible bias current. The input offset voltage is unimportant if the current I_i is supplied from a current source; but, if I_i comes from a voltage source through a resistor R_i, then the offset voltage of the amplifier is the main limiting factor for accuracy and dynamic range.

Fig. 4.5.2:

Circuit diagram of converter.



We now refer to the detailed circuit diagram. The diagram is similar to one of those discussed in the Linear Applications Handbook of National Semiconductor. The 331 uses a single power supply, and the pins should not be driven negative. Diodes D4 and D5 protect pin 7 from any possible negative swing of the operational amplifier output. The reverse current of the diodes is returned to ground by R16, thus not perturbing the measurement. The voltage V_{comp} to the 331 comparator is obtained from the power supply through the R9-R10 divider. Diodes D1-D3 together with P1-R2 compensate for temperature variations; the value of the total resistance is usually around 450K. The R6 resistor contributes to a slight improvement

of linearity. Potentiometer P3 is used to null the amplifier offset voltage. This nulling is important in situations where the current to the 356 inverting input comes from a voltage source through a resistor. To emphasize this point we include in the present diagram an input current to voltage converter where no correction for offset voltage of the operational amplifier is made. (The input amplifier has a bias current of the order of 1 pA and can be used with very large resistors.)

Potentiometer P2 is used to adjust the scale factor by adjusting I_{ref} . The pot and R3 together with R4 actually determine the I_{ref} (not just R4). With the components shown, the one-shot pulse width is close to 80 μs ($=1.1 \cdot R_{11} \cdot C_2$). An input current of 10 μA will produce a frequency of 1 kHz with a reference current of about 130 μA.

If one is interested in integrating a small voltage then a low offset voltage drift amplifier is to be used. For example, the OP-07 is suitable operational amplifier for most of these applications. A circuit with adjustable voltage gain from 10^2 to 10^3 is shown in Fig.4.5.3. This is the circuit for which the ready-made pcb has been prepared. The circuit should be adjusted and tested for output frequencies from 10 Hz to 10 kHz.

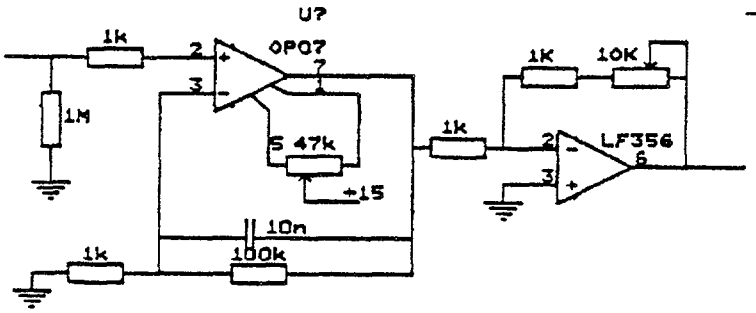


Fig. 4.5.3:

Low drift voltage amplifier.

Notes:

PART FIVE

RADIATION DETECTORS

Radiation detectors - an introduction.

The experiments in this chapter are designed to expose the students to a few of the radiation detectors, signal processing techniques, and applications of nuclear systems that they may encounter after the course.

It is important when designing or maintaining any instrumentation system to, first, have a thorough understanding of the system; that is what is the purpose and function of the equipment or system? Second, one must understand the operation of the transducers (in this case the radiation detectors) that actually make the measurement. One must understand the type of signal generated by the detector and how the signal must be processed and finally analyzed. Only with this background information can a system be studied and the signal processing functions logically broken down into small steps, the path of the signal traced through the system, and the input and output signals checked for the proper operation of each subsystem or component.

Because this manual has been prepared primarily for an electronics course, only a limited amount of time is available for demonstrating nuclear measurements. Also, because of the wide variety of applications and the cost of the various nuclear instruments, it is impossible to demonstrate all of the systems and processing techniques that the students will encounter after the course. Therefore, only a few experiments have been selected for this course; each combining or demonstrating a variety of detectors and signal processing techniques.

The experiments in this chapter differ greatly from the usual set of experiments found in many nuclear physics or nuclear engineering laboratories. Rather than concentrate on the properties of nuclear radiation, these experiments will attempt to demonstrate the operation of detector systems, several advanced methods of processing the detector signals, methods of analyzing the signals, and methods of verifying the manufacture's specifications for the individual modules and systems.

Overview

RADIATION DETECTION

REVIEW

All radiation detectors depend on the ionization or excitation of atoms produced by radiation. In many detectors, the charge from the ionization process, either electron - ion pairs in gases or electron - hole pairs in solid state detectors, is collected and becomes the output signal. In scintillation detectors, the light photons emitted when excited electrons in the atoms drop down to a lower energy states are collected and then converted to electrical charge at the photocathode of the photomultiplier tube. The charge is then amplified in the photomultiplier tube and the amplified signal is the output from the anode.

The ionization/excitation process is statistical in nature. It involves many interactions between a charged particle and the atomic electrons and although the average energy per electron - hole or electron - ion pair can be determined fairly accurately, the total number of charge pairs will vary from event to event even though the incoming radiation may be monoenergetic and deposits the same amount of energy each time. However, the incoming radiation may not deposit all of its energy in the detector. For example, photons (gamma rays and x-rays) interact in matter by three different mechanisms; photoelectric, Compton scattering, and pair production. In photoelectric events, the photon essentially transfers all of its energy to an atomic electron; knocking the electron out of the atom and giving it kinetic energy. This photoelectron then proceeds to lose its energy by ionizing/exciting other atoms. If the event occurs near the edge of the detector, the photoelectron may lose only part of its energy in the active region and the rest in the walls of the detector. The result is that only part of the energy of the incoming photon is available for producing ionization/excitation in the detector. Compton scattering results in the photon transferring only part of its energy to an atomic electron and a scattered photon of lower energy also being emitted. This secondary photon may escape from the detector. Thus only part of the energy of the original photon is deposited in the detector to produce ionization/excitation. Similarly, pair production (possible only if the incoming photon has an energy greater that 1 MeV) may also deposit only part of its energy in the detector.

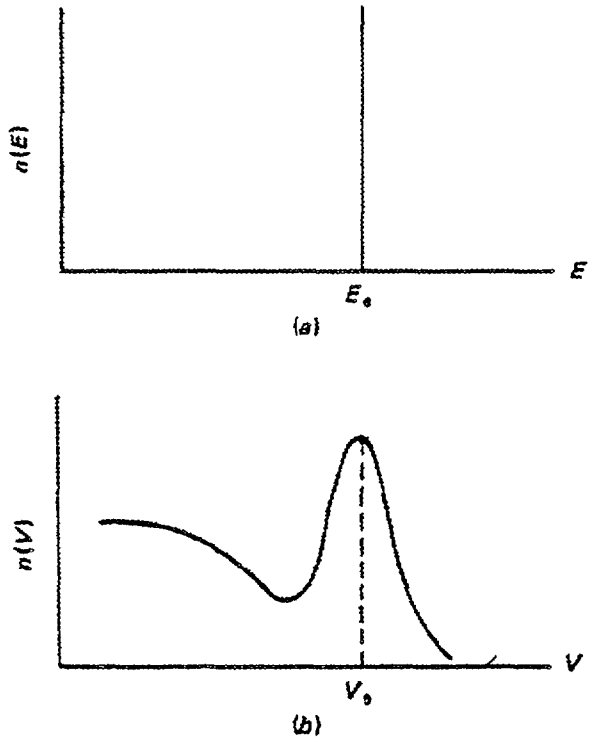
A. ENERGY SPECTRA

Energy spectra are simply plots of the number of events vs. the energy of the events. In nuclear spectroscopy, two types of spectra become important; source spectra and detector or measured spectra. A source spectrum is the plot of the number of radiations from a source as a function of the energy of the radiations. For alpha sources, gamma-ray sources, characteristic x-ray sources, and a few others, the source spectra will consist of a series of lines since these radiations are monoenergetic. With other sources, such as beta sources, the source spectra may be a continuous distribution from zero energy to some maximum energy or in the case of beta spectra the endpoint energy of the nuclear decay.

The detector or measured spectrum is the measurment of the number of events occuring in the detector plotted as a function of the pulse height (note that the pulse height is usually

Fig. 5.1:

Typical spectrum



proportional to the energy deposited in the detector by the radiation). No detector and electronic system is perfect and will introduce noise and in the case of nuclear detectors statistical variations into the signal being detected. Because of the variety of ways by which radiation interacts with matter the measured spectra sometimes has little similarity to the source spectra.

A typical source spectrum for the gamma ray from a Cs-137 source is shown in part(a) of Fig.5.1. Part (b) shows a corresponding detector spectrum with the output voltage Vo corresponding to the energy of the monoenergetic gamma ray. Note the broadening of the peak due to the random statistical processes and noise in the detector and electronic system. Note also the low energy tail corresponding to the partial energy events when only pat of the gamma-ray's energy is deposited in the detector.

The problem in nuclear spectroscopy is to infer the source spectrum from the measured spectrum. In order to do this one must understand all of the factors including radiation interactions, detector characteristics, signal processing, and the analysis of the spectra performed by the analyzer or computer programs.

B. RESOLUTION

One of the important parameters frequently used to judge the quality of detectors is resolution. Alpha particles and most photons (gamma rays and charactistic x rays) are monoenergetic. This means that in a plot of the number of radiations vs the energy, the plot is a straight line as shown in Fig. 5.1. However, because of the statistical nature of the ionization/excitation processes and the radiation interactions in matter as discussed in the preceding section, the peak in the spectrum will be broadened. In addition, electronic noise from the pulse amplification and processing systems will also contribute to a broadening of the peak. The result may, therefore, look like the measured spectrum shown in Fig. 5.1.

The resolution of the detector is a measure of the width of the peak. It is defined as the full width of the peak at one half of the maximum height (full width at half maximum height,

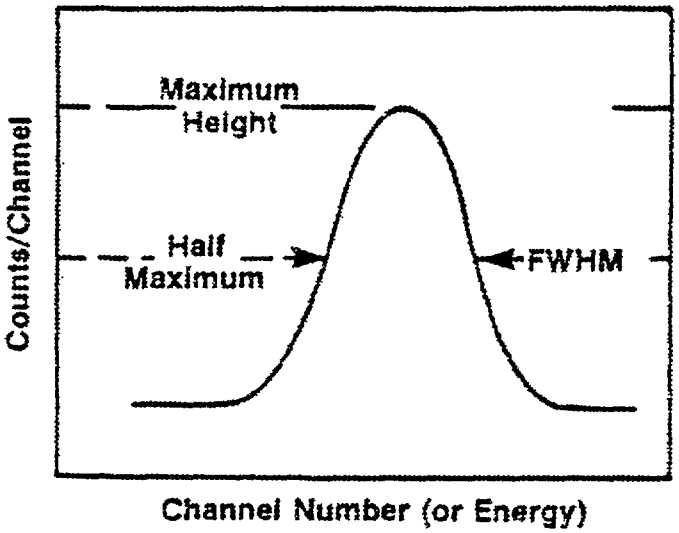


Fig. 5.2:

Resolution

FWHM). The FWHM is given either in energy or when divided by the energy of the peak and multiplied by 100 is expressed as percent resolution. The process of determining the resolution may be complicated if the peak is sitting on a background due to either background radiation or partial energy events such as Compton scattering by higher energy photons. In this case, the height of the peak is determined by approximating the underlying base with a straight line and measuring the height as the distance from the base line to the highest point of the peak. See Fig. 5.2. It can be seen that the resolution is a measure of the ability of a detector and system to determine the energy difference between two peaks. Thus, when trying to identify different radioisotopes by measuring the energy of the radiation emitted, the resolution of the system becomes very important.

The factors determining the resolution of a detector include:

- the type of detector,
- the size of the detector, and
- quality of the detector.

The resolution of a particular detector is also usually dependent on the bias voltage. Therefore, it is important to understand how variations in the bias voltage affect the resolution and operation of the detector and how to determine the optimum operating voltage for any system.

C. DETECTOR EFFICIENCY

Three types of detector efficiencies are commonly used; absolute, intrinsic, and absolute peak efficiency. Absolute efficiency is defined as the number of events recorded divided by the number of radiations emitted by the source. In this case, the number of events recorded is the sum of all of the pulses from the detector, from zero pulse height to the maximum pulse height. Note also that this definition depends on the solid angle that the detector presents to the source and is strongly dependent on the source detector distance, especially when the source is close to the detector.

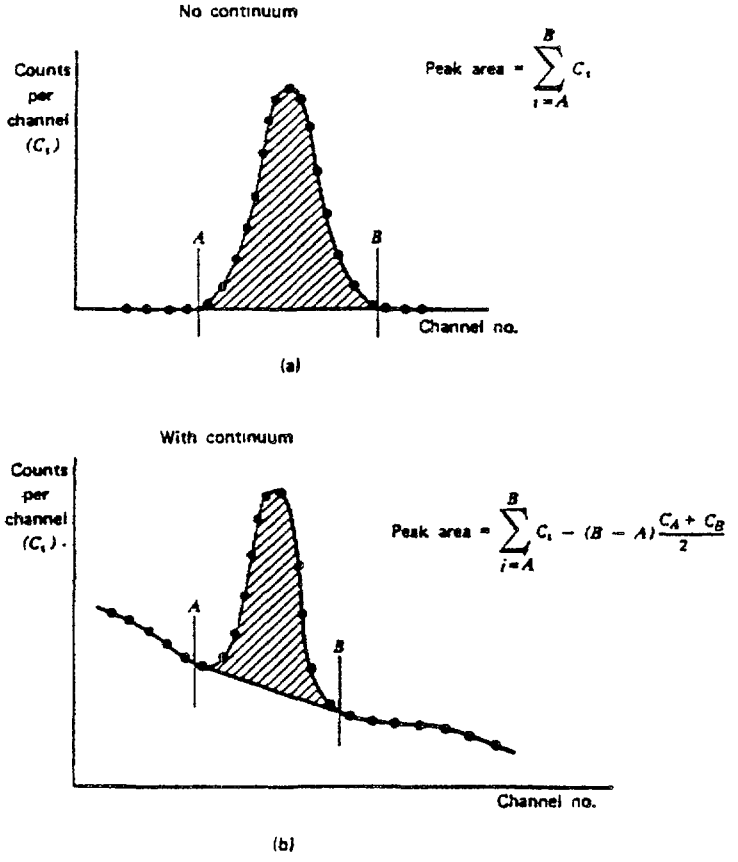
Intrinsic efficiency is defined as the number of events recorded divided by the number of radiations incident on the detector. One might think that the intrinsic efficiency should be independent of the source detector geometry but if one defines the detector as the outside

of the cover instead of the active region, then there may still be some dependence on the source detector separation.

Peak efficiency is defined as the number of events recorded in the peak compared to the total number of events recorded. One is usually concerned with the absolute peak efficiency which is defined as the number of events recorded in the peak divided by the number of radiations emitted by the source. Note that here one is concerned with the

Fig. 5.3:

Peak areas.



total number of events in the peak, or the area of the peak, not just the height of the peak. In simple, well isolated peaks, the area of the peak is determined by just summing the counts in all of the channels in the peak. In practice, since the peaks may sit on background or the partial energy events from higher energy radiation, this "background" must be determined and subtracted from the sum of the total number of counts in the peak channels. Again, the simple method is to just draw a straight line representing the background under the peak, determine the number of counts below the line, and subtract these counts from the sum of the counts in the peak region. See Fig. 5.3. The process of determining the area of the peak may become very complicated, especially if two or more peaks overlap.

The efficiency of a detector depends not only on the size of the detector but also on the energy of the radiation. The low energy efficiency is often determined by the absorption of the radiation in the material used in the detector housing or the material that separates the source from the active region of the detector. The high energy efficiency is often determined by the thickness and size of the detector; high energy photons may pass through the detector without any interaction. The efficiency of a system is often one of the important parameters used in setting the cost of a system and is one of the parameters that must be frequently measured, especially in experiments where the absolute number of events must be determined.

D. DEAD TIME

Dead time, sometimes called the resolving time, of a system is a measure of a system's ability to distinguish between two separate events in time. Some detectors such as the G-M detector are dead to any event arriving within the dead time of the tube; that is there will be no signal out of the detector for the second event. In most linear systems, the two events will simply be added together in the detector to give one output pulse since the detector does not know whether the energy deposited comes from one event or two. In this case the height of the output pulse will correspond to the sum of the energies deposited by the two separate events. These summing events can give rise to additional peaks (sum peaks) in a spectra as well as distorting the shape of the peaks.
In simple systems consisting of a detector, amplifier, and counter, the dead time is frequently determined by the detector. In simple spectroscopy systems, the slowest component is frequently the MCA. In more complicated systems where the detector signal may be processed by optical feedback preamplifiers and/or pulse pile-up rejectors, each different component may contribute to the dead time of the system.

E. CLOCK TIME(TRUE) / LIVE TIME

Clock time or true time is the time that a system operates as determined by an independent clock such as the clock on the wall or the operators wrist watch. However, the system is not always available for detecting and analyzing events because of the detector dead time or dead time in the signal processing system. The first stage of the ADC is a gate which is closed as soon as the ADC starts to process a signal. This stops a second pulse, if it arrives shortly after the first pulse, from interfering with the analysis of the first pulse; the second pulse will be lost (that is, it will not be analyzed and recorded). The time that the system is actually available for accepting an event (the input gate is open) is called the live time.

Most MCA systems can be preset either for a given clock time or for live time. In addition, many MCA systems will have special inputs for signals from signal processing modules such as pile up rejectors (PUR) and will correct for the dead time introduced by these systems.

F. PILE-UP REJECTOR

Pulse pile up can occur if two closely spaced events combine to form one distorted pulse. Pile-up rejectors (PUR) inspect the shape of the pulses and discard those whose shape is distorted due to pile up. Pulse pile-up rejectors become very important in those systems operating with very high counting rates. Pulse pile-up rejectors greatly improve the shapes of the peaks in a spectrum recorded at high counting rates, but also contribute to the dead time of the system. Correction for this increased dead time is discussed in section E.

Notes:

EXPERIMENT 5.1

CHARGED PARTICLE SPECTROSCOPY

OBJECTIVE

Several different silicon detectors for charged particle spectroscopy will be studied. The important properties such as resolution and voltage dependence will be investigated as well as the influence of the electronic system on the quality of the spectra.

REVIEW

A solid state detector can be considered as a simple ionization chamber with the gas replaced by a solid. This presents two advantages:

- the energy required to produce a charge carrier (electron-hole pair) is only 3.62 eV in silicon (improved resolution) and
- the range of the charged particles is very short in solids so the particles can deposit all of their energy in the active region of the detector.

A silicon charged particle detector is a wafer of silicon having surface contacts forming a p-n junction. These contacts may be very thin surface contacts such as on the surface barrier (SB) detectors, material diffused into the silicon to form a junction (diffused junction detectors, DJ), or passivated, ion implanted contacts such as on the passivated implanted planar silicon (PIPS) detector.

A reverse bias voltage is applied across the contacts to form a depletion region with no free charge carriers. When radiation interacts in the depletion region, creating electron-holes pairs, the electric field from the reverse bias voltage sweeps the electrons to one terminal and the holes to the other. This output charge pulse is then integrated and amplified in a charge sensitive preamplifier to produce a voltage pulse.

The thickness of the depletion region will depend on the applied bias voltage. The higher the voltage, the thicker the depletion region and the more energy a particle can deposit in the detector before passing out of the active or depletion region. This is usually not important for detecting alpha particles but may become important when trying to detect less ionizing particles such as beta particles or very high energy particles that one might produce with a particle accelerator. The leakage current is also directly dependent on the applied bias voltage and the higher the voltage, the larger the leakage current. Thus the optimum voltage is one that will produce efficient charge collection, maximum thickness of depletion region, but not excessive leakage current.

The noise introduced by the preamplifier is strongly dependent on the input capacitance. The detector can be considered as a parallel plate capacitor; thus the larger the area of the detector or the thinner the depletion region, the larger the detector capacitance and the more noise the preamplifier will introduce into the system. Although the preamplifier design can be optimized for a given input capacitance, the smaller the value of the input capacitance the better. With this in mind, it should also be obvious that the preamplifier should be placed as close to the detector as possible to minimize the capacitance that might be introduced by a long coaxial cable. ORTEC recommends a maximum cable length of 50 cm for the preamplifier that will be used in this experiment.

WARNINGS:

Whenever you pump down or let the chamber up to air, it is imperative that the bias supply be turned off. Most detectors are sensitive to light and, therefore, the bias voltage should never be applied to the detector unless the vacuum system is closed.

Completely discharge the detector bias circuit before connecting anything to the Detector Input connector on the preamplifier. To discharge the detector bias circuit, short circuit the Detector Bias input on the preamplifier to ground for a least 20 seconds or if a variable supply is use, simply turn the voltage control to zero and leave it for 20 seconds. DO NOT SHORT the Detector Input connector to ground.

Be careful not to touch the face of the detector with your fingers. Some detectors have a thick covering or are fabricated in such a way that the surface can be cleaned, but many detectors will be ruined.

If you have to open the preamplifier, be very careful not to touch either of the two high value resistors. Oil from your fingers will increase the leakage current on the surface. If they must be cleaned use methanol only.

EXPERIMENT **Experiment 1**

Connect the spectrometer as shown in Fig.5.1.1.

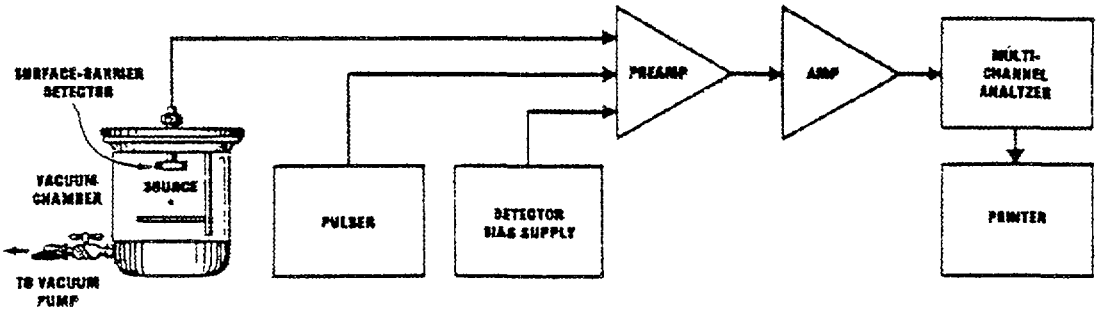


Fig. 5.1.1:

Alpha spectrometer.

(i) Using one of the PIPS detectors, locate the Am-241 alpha source about 1 cm from the face of the detector. Evacuate the chamber and turn on the bias voltage to the value recommended by the manufacturer. Adjust the gain of the main amplifier so that the largest peak in the Am-241 spectrum is located in approximately channel 3500. Record a spectrum for at least 1000 seconds. Americium-241 has five peaks in its spectrum. A semi-log plot of an Am-241 spectrum is shown in Fig. 5.1.2. Many detectors, depending on their resolution are not capable of resolving all five peaks.

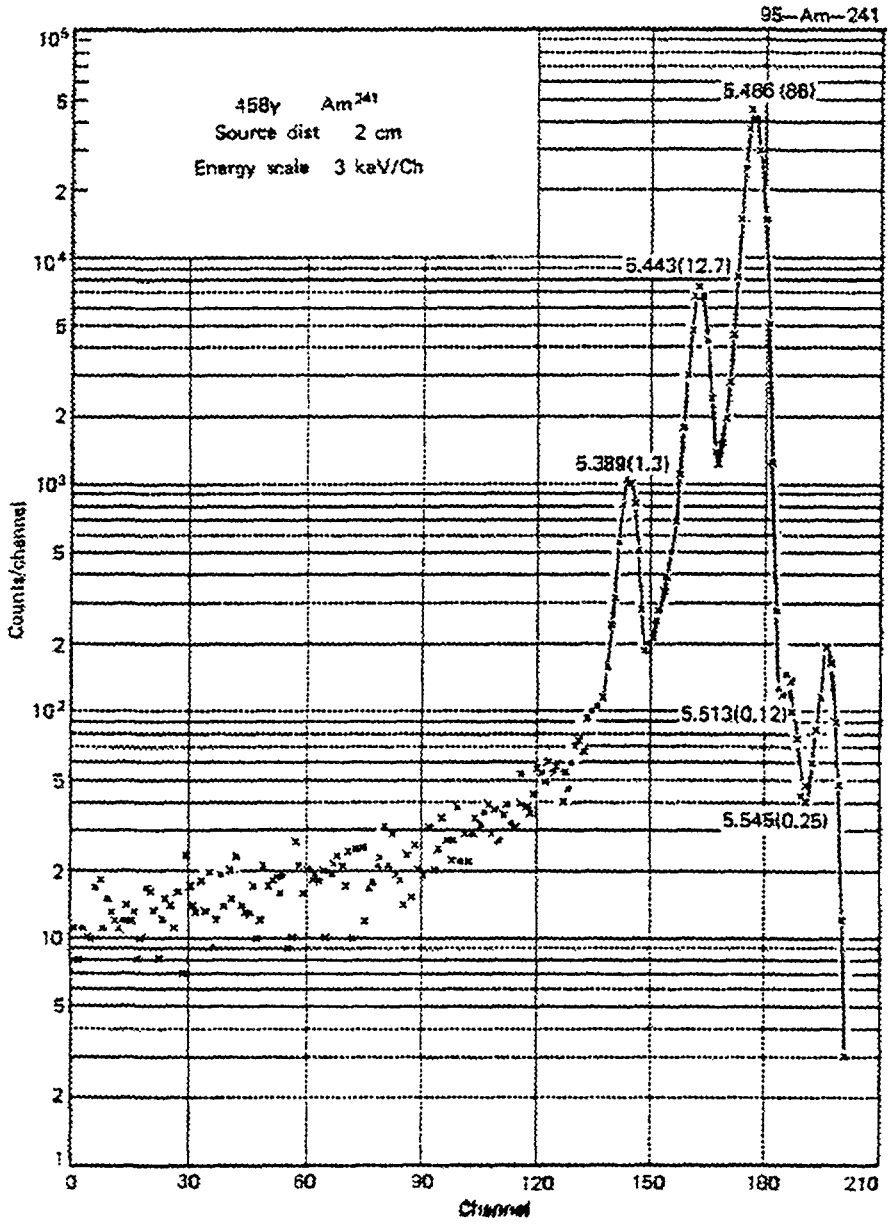


Fig. 5.1.2:

Am-241 spectrum.

How many peaks to you see in your spectrum? Using a Region Of Interest (ROI), determine the total number of events registered in the spectrum. Record this number.

Using the two largest peaks at 5.486 and 5.443 MeV, determine the energy calibration of the system. This energy calibration is usually not a very good calibration because the two points are too close in energy; it is always best to have the calibration points spread out to cover the entire energy range of interest.

(ii) Calibration using a pulser. A second method of calibrating the system is to use a pulser. Connect one of the Ortec model 480 pulsers to the test input of the preamplifier. Use the attenuated output from the pulser. Set the helipot control to 549/1000. This control is a ten turn potentiometer with each complete turn of the control subdivided into 100 parts. Therefore, the control can be set to 1/1000 of the full range. Now, using the attenuator switches and the 22 turn calibrate control (adjusted with a screwdriver), adjust the pulser so that the center of the peak from the pulser falls in the same channel as the

5.486 MeV peak from the Am-241 source. The pulser is now calibrated in MeV with 100 corresponding to 1 MeV, 200 to 2 MeV, etc. Record a spectrum using the pulser adjusted to 100, 200, 300, 400, 500, and 600. Determine the energy calibration of the system and the zero intercept of the energy calibration. What channel number is equal to zero energy? How does this compare with the value from the energy calibration in part i?

(iii) Determine the FWHM of the 5.486 MeV peak in the Am-241 spectrum in energy. How does this compare with the value reported on the certification sheet supplied with the detector?

(iv) Decrease the bias voltage by 25 volts and record a spectrum. Determine the resolution of the 5.486 MeV (note that you will probably have to do another energy calibration; use the two large peaks in the spectrum for the calibration). Did the location of the peaks and the resolution of the system change? Decrease the bias voltage another 25 volts and repeat? What conclusions can you make about the effect of the bias voltage on the energy resolution of the detector? Can you explain why the resolution and energy calibration of the detector is a function of the bias voltage?

(v) Turn off the bias voltage and open the vacuum system to the air. Move the source closer to the detector (0.5 cm). Evacuate the chamber, apply the recommended voltage and again record a spectrum. Determine the resolution of the 5.486 MeV peak and compare with the previous measurements. Repeat with the source-detector distance equal to 1.5 cm. How does the source-detector distance affect the resolution? Why?

(vi) Return the source-detector distance to 1 cm, but cover the source with a single layer of plastic wrap. Record a spectrum and determine the location of the major peak in the Am-241 spectrum. Using the energy calibration from part (i) or (ii), calculate the energy of the alpha particles after they have passed through the plastic. How much energy did they lose? How did the resolution change? Using a ROI, determine the total number of alpha particles detected and compare with the total number of alpha particles detected in part i (remember to correct for any differences in the counting times). This spectrum is more typical of the alpha spectra normally seen, since most sources are either thick sources or have a thin protective covering over them. If the alpha source is a thick source such as when counting a "wipe", the spectrum will produce alpha particles from zero energy to the maximum energy of the source, depending on where in the source the alpha decay occurred. If the decay occurred on the surface, then the alpha particle will have its full energy, but if the decay occurred deep in the source, it may lose all of its energy in the source and never get out of the source. Thus, most alpha spectra will have alphas from zero energy to the maximum energy from the source, and most detectors are not used for spectroscopy but only for counters to detect and count the number of alphas.

Experiment 2

(i) Calculate the charge, Q, produced in the detector by a 5 MeV alpha particle. It takes 3.62 eV of energy to produce an electron-hole pair in silicon and each electron or hole will carry 1.6 E -19 Coulombs of charge, so

$$Q = \frac{5 \cdot 10^6 \text{ [eV]}}{3.62 \text{ [eV/charge]}} \times 1.6 \cdot 10^{-19} \text{ [Coulombs]}$$

The Ortec preamplifier has a test input that will accept a test pulse with a fast rise time and long decay time (typically the rise time is less that 10 nanoseconds and the decay time greater that 200 microseconds). This will approximate a step pulse to the

preamplifier. The input capacitor in the preamplifier is 1 picofarad, so the charge delivered by the test input to the input of the preamplifier is given by

$$Q = V \cdot C = V \cdot 1.0 \cdot 10^{-12}$$

(ii) Using a "T" connector on the attenuated output of the ORTEC Model 480 pulser, connect one lead to the test input to the preamplifier and the other to an oscilloscope. Using the scope, measure the amplitude of the pulse corresponding to the 5.486 peak in Am-241. Calculate the input charge from the pulser to the detector. Compare this with the charge produced by 5.486 MeV alpha particle.

(iii) Without a source in the vacuum chamber, but with the bias voltage applied to the detector, accumulate a spectrum using the pulser. Using the energy calibration from the earlier measurements calculate the resolution of the system for the pulser peak. This is the noise or contribution to the resolution introduced just by the electronics system, primarily by the preamplifier. In general, the noise is added in the following way:

$$(\text{FWHM})^2_{\text{total}} = (\text{FWHM})^2_{\text{detector}} + (\text{FWHM})^2_{\text{electronics}},$$

where the noise from the detector is caused by statistical variations in the number of charge carriers created, incomplete charge collection, leakage currents (both bulk and surface), and Johnson noise from the detector contacts. Does the electronics system contribute significantly to the overall resolution of the complete system?

Experiment 3

Determine the resolution of the other silicon detectors supplied for the experiment. For each detector place the source 1 cm from the detector and using a ROI, determine the total number of counts recorded and compare the counting efficiency of the detectors. Make a table showing the type of detector, the area of each detector, the resolution and the counting efficiency.

Notes:

Experiment 5.2

SCINTILLATION DETECTORS

Several different inorganic scintillation detectors will be studied with the aim of determining their properties and behavior under various experimental conditions. The resolution, efficiency and timing properties of the detectors will be examined and the shape of the pulses coming from the preamplifier will be investigated.

OBJECTIVE

There are a number of organic and inorganic materials that can be used for scintillation detectors. The most frequently used material is the NaI(Tl).

REVIEW

The important properties of a NaI (Tl) detector are summarized below.

1) TYPE OF RADIATION DETECTED.

The NaI(Tl) detectors are used in gamma and x-ray spectrometry. For gamma rays, the detectors are usually cylindrically shape; a common size being 5 cm in diameter and 5 cm high. The "standard" detector has a diameter of 7.5 cm and height of 7.5 cm. Larger and smaller detectors can be ordered. For detection and analysis of x-rays, the detector has the form of a thin (1 or 2 mm) disk, with a 1 cm or larger diameter.

2) RESOLUTION.

In scintillation detectors, the resolution is expressed in percent. For gamma-ray detectors, FWHM of the 661.9 keV Cs-137 peak is determined in keV. The value is divided by 661.9 and multiplied by 100. A good NaI(Tl) detector has resolution better that 7 %. A detector with resolution above 12 % is considered to be poor.

For x-ray scintillation NaI(Tl) detectors, the resolution is also expressed in percent, measured usually with the Cd-109 source (emitting x-rays of Ag, at energies of 22.1 and 25.0 keV). A resolution of 20 % is acceptable.

3) EFFICIENCY.

The NaI(Tl) detectors are very efficient for detecting gamma rays in the energy range around 100 keV. Low energy gamma rays are not seen because they cannot penetrate the walls of the detector housing. On the high energy side, the detectors becomes less sensitive; larger detectors detect high energy gamma-rays better than small. X-ray NaI(Tl) detectors are 100% efficient in the energy range around 30 keV; at higher and lower energies the efficiency decreases.

Nowadays, NaI(Tl) detectors are normally sold as integral (monolithic) assemblies, including the NaI crystal, the photomultiplier tube, and the magnetic shield, all in a stainless steel or aluminum housing.

A scintillation material particularly useful for measuring high energy gamma-rays is BGO (bismuth germanate). Due to the high atomic number of its components, it efficiently stops the high energy gamma rays. It has poor resolution (about 16 %) but excellent efficiency.

NOTE: The high voltage power supply for NaI(Tl) detector assemblies should be able to deliver at least 2000 V and 1 mA. Although many photomultiplier tubes operate at 1000 volts, some systems require 1600 V for optimum resolution. The high voltage power supplies intended for semiconductor detectors usually cannot be used for scintillation detectors because of the current requirements.

Experimental setup.

EXPERIMENT

Two NaI(Tl) detectors for gamma rays (5 x 5 cm and 7.5 x 7.5 cm), and an x-ray detector will be studied and compared to a 5 x 5 cm BGO detector. For all of the detectors, the same high voltage supply, amplifier and MCA will be used in an arrangement as shown in the diagram below. The signals from the preamplifier or directly from the anode of the photomultiplier will be observed with the oscilloscope. The spectra will be accumulated in a MCA card installed in an AT computer.

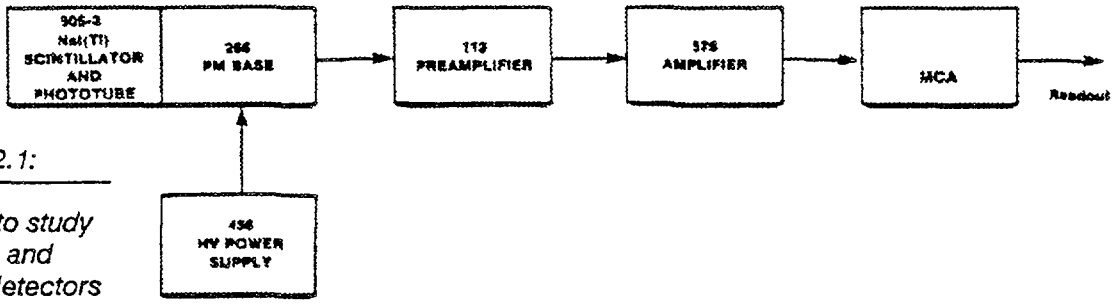


Fig. 5.2.1:

Setup to study NaI(Tl) and BGO detectors

Before starting the experiment, become familiar with the operation of the MCA. Learn how to collect a spectrum, store it, how to calibrate the system and how to determine the values that characterize the peaks.

Check if the high voltage supply is correctly calibrated: measure the voltage, and compare with the setting on the dials. Be careful about the type of voltmeter to be connected to the output of a high voltage power supply.

Check the operation of the amplifier and MCA by using a pulser. A signal with suitable shape (short rise time- 10 ns, long fall time - 200 μs) should be fed to the amplifier input. The amplified signal are recorded in the MCA; if the setup is optimized, the peak will be not more than two channels wide. Change the amplitude of the input pulses in defined steps, and observe the positions of the peaks in the spectrum. This will tell you if the system is linear.

Experiment 1: Influence of high voltage on the resolution and position of the peak.

(i) The 5 x 5 cm NaI(Tl) detector, with a preamplifier, should be connected to an amplifier and the MCA. Observe that the signal on the unipolar output of the spectroscopy amplifier is in fact bipolar. Explain this observation.

(ii) Set the high voltage to the value recommended by the manufacturer in the certificate supplied with the detector. Place the Co-60 and Cs-137 calibration sources in front of the detector, at a distance such that the counting rate of the detector will be about 2000 counts per second. If no counter is available, how do you determine this counting rate using a MCA analyzer?

(iii) Adjust the gain of the amplifier so that the 1332 keV peak of Co-60 will be in channel 900 of a 1024-channel analyzer. Cobalt-60 emits two gamma rays with energies of 1173.2 and 1332.5 keV, 99.9 and 100 percent of the time.

(iv) Record a spectrum, with a preset time sufficient to collect at least 10,000 counts in the smallest peak of interest.

(v) Perform an energy calibration, and determine the FWHM and resolution of the Cs-137 and Co-60 peaks. Record the positions of the peaks (in channel numbers).

(vi) Repeat the steps (iv) and (v) with high voltage values decreasing in steps of 50 V, until all the spectrum is collected in the first 100 channels of the MCA. At each value of high voltage setting, record the positions, FWHMs and resolution of the peaks.

(vii) Plot the resolution (in percent) of the Cs-137 peak as a function of the applied voltage. What is the operating voltage for the best resolution?

(viii) In their operating range, the gain of photomultiplier tubes is reported to vary as the seventh power of the applied high voltage. Plot the log of the channel number of the Cs-137 peak vs the log of the high voltage and determine the slope of the resulting line. Is the value of the slope approximately equal to seven?

Experiment 2: Comparison of different detectors.

(i) Start with the 7.5 x 7.5 cm NaI(Tl) detector. Using a mixed isotope source adjust the counting rate of the system to about 2000 counts per second. Record a spectrum and using the features of the MCA, determine the areas of the Cs-137, Co-60, and Y-88 peaks. Measure and record the source-detector distance used in this experiment. Yttrium-88 emits two gamma rays with energies of 898.0 and 1836.1 keV, 94.1 and 99.4 percent of the time.

(ii) Using the same source-detector distance as in part i, accumulate spectra with the 5 x 5 cm NaI(Tl), and BGO detectors. Adjust the high voltage and amplifier gain so the peaks are approximately in the same channels for each of the spectra. Prepare a table showing the areas of the three isotopes, taken by different detectors. This table will give you an indication of how the absolute peak efficiencies vary with the detector size and type.

Experiment 3: X-ray NaI detector.

(i) Connect the x-ray NaI(Tl) detector, and collect a spectrum using the Am-241 source. Adjust the gain (or high voltage, or both) of the system in such a way that all the peak will be clearly displayed. Calibrate the MCA.

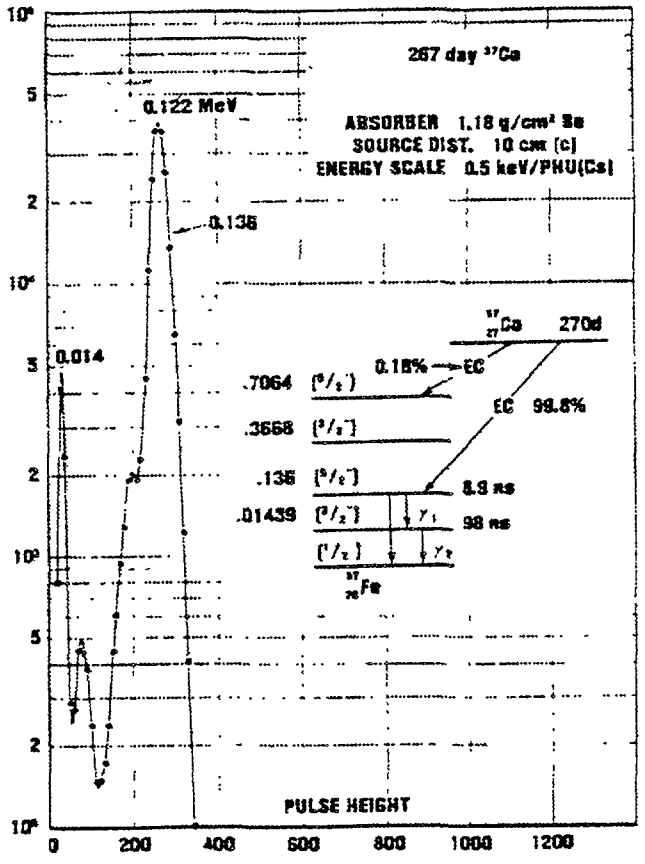


Fig. 5.2.2: Co-57 spectrum.

(ii) Determine the resolution of the detector at the energies corresponding to the Co-57 gamma rays. For orientation, a spectrum of Co-57 is shown in Fig. 5.2.2.

(iii) Collect several spectra using different x-ray sources; including the Ba-133. Try to make some conclusions about the efficiency of the detector at the different x-ray energies.

Experiment 4:

(i) Instead of the tube base with the preamplifier, install the tube base alone. The signal is now taken directly from the high voltage capacitor in the tube base. With the oscilloscope observe the shape (rise time, fall time, width, and height) of the signal.

(ii) Turn off the high voltage and open the tube base. Find the value of the resistor connected between the anode and the high voltage terminal. Parallel this resistor with another one of about the same value; close up the tube base and restore the high voltage. Observe the signal again; note the change in signal size and duration.

Remove the extra resistor from the circuit.

(iii) Using a "T" connector at the input of the oscilloscope, terminate the open connector with 2K resistor. How does this effect the pulse shape from the photomultiplier tube? Explain why the change occurs.

EXPERIMENT 5.3

HIGH RESOLUTION GAMMA DETECTORS

OBJECTIVE

The operation of a pure (intrinsic) germanium detector will be studied in detail. The influence of the electronic system on the shape and quality of the gamma spectrum will be investigated. The important properties of the detector will be determined: resolution, peak shape, and efficiency, as a function of gamma ray energy and counting rates.

REVIEW

A high resolution gamma detector is a properly shaped piece of ultrapure germanium. Different forms of pure Ge detectors are available, and some of them are shown in Fig.5.3.1. The surfaces are prepared in such a way that they make electrical contacts. High voltage is applied to these electrodes, anywhere between 2500 and 5000 V. In absence of radiation, and cooled to a low temperature, the very pure Ge is an almost perfect insulator. The current through it, with high voltage applied, is in the range of picoamperes.

When gamma rays are stopped in the detector, they produce charges (electrons and holes) which are collected by the electrodes. The charges are collected in a capacitor, and processed by a charge sensitive preamplifier.

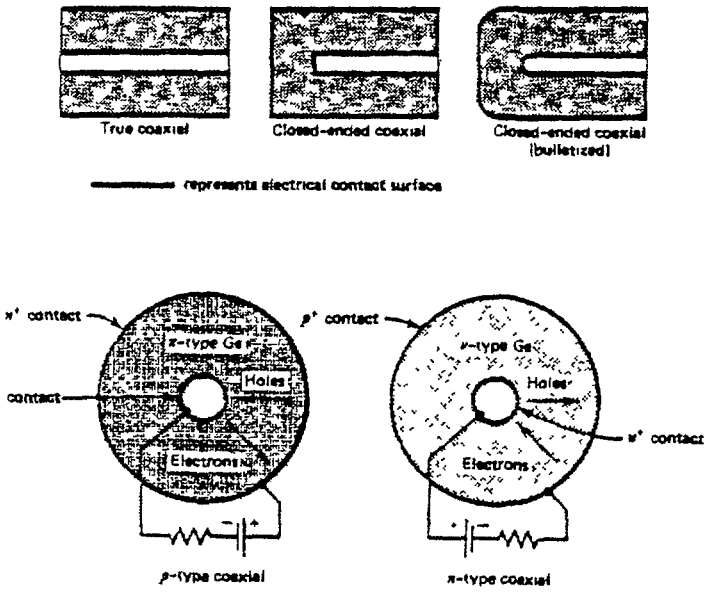


Fig. 5.3.1:

Different shapes of Ge detectors.

In a typical resistive feedback preamplifier we should observe the following components:

- the first stage of the preamplifier is a FET located inside the cryostat, i.e. operating at low temperature,
- a test input is available; the test signal can be applied to the FET input,
- the high voltage is not connected to the detector directly but via a filter consisting of high value resistor and a capacitor; this prevents the operator from making the mistake putting high voltage on the detector in a steplike manner and ruining the input FET. The time constant of the filter assures that the voltage is applied gradually.

The amplifier to be used in the experiment can shape the signal in a classical Gaussian shape, or it can operate as a gated integrator. At low counting rates, Gaussian shaping should be selected. At high counting rates, the gated integrator circuitry has several advantages.

The multichannel analyzer is in the form of an add-on card for an PC computer. Such MCAs are less expensive than the classical stand-alone devices, and offer several advantages in way of data manipulation; they are fully adequate for most of the problems encountered in applied nuclear studies.

Experimental setup

EXPERIMENT

Assemble a gamma ray spectrometer by connecting individual electronic units, as shown in Fig.5.3.2.

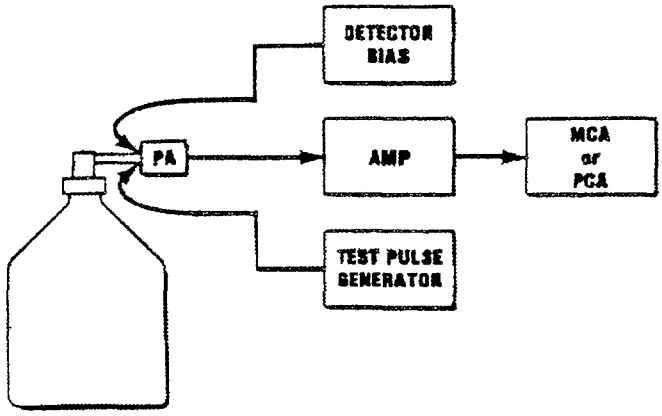


Fig. 5.3.2

Block diagram of a Ge spectrometer.

If the spectrometer is to be grounded, this should be only at one point; as close to the preamplifier as possible. Take care that all the cables are working properly. An oscilloscope is essential for proper setup of the equipment.

In the determination of the FWHM as a function of counting rate and shaping time, we will follow the recommendation of Fairstein (E. Fairstein, IEEE Trans. Nucl. Sci NS-32(1), p31, 1985). The FWHM will be determined at different values of the t (t is approximately the shaping time as set on the front of the amplifier; it can be better defined by observing the signal with the oscilloscope (see Fig.5.3.3) at a selected counting rate. The FWHM of the 1332 keV peak should be measured at five points (values of t) or more at each counting rate. The counting rate should be changed, to obtain a family of curves, showing the dependance FWHM on t for different counting rates. This approach offers the following

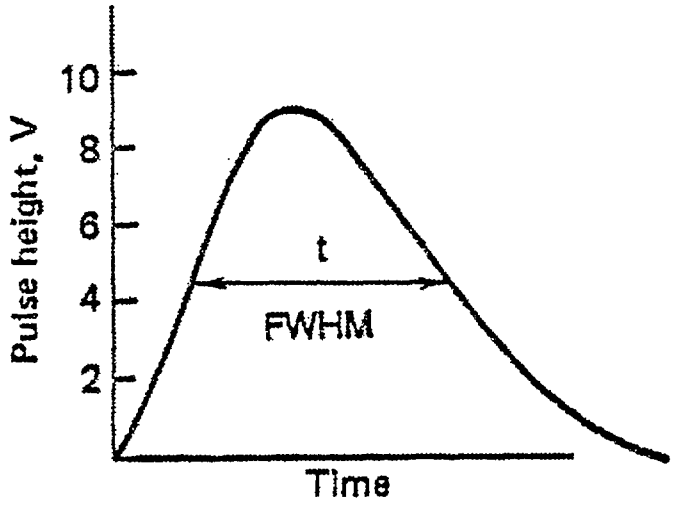


Fig. 5.3.3:

Specifications of a nuclear pulse.

advantage: for any counting rate, the best shaping time can be selected for the real experiment, giving the best possible resolution.

The main properties of the calibrated isotopic sources used in the experiments are summarized in Table 5.3.1.

Experiment 1

Before starting the measurements, install the MCA board, and become familiar with its operation. The installation of the board involves placing it in one of the free slots of the computer. The software should be copied to the hard disk of the computer. The MCA card should be set to operate with 4096 channels.

The MCA is fully controlled from the computer keyboard. Learn the most essential functions, such as moving the cursor, setting regions of interests (ROIs), calibrating the spectrum, and determining the peak position, FWHM, and area.

In the first part of the experiment, the resolution of the detector will be determined at the recommended values of high voltage and shaping time constants, to check the data given in the certificate for the detector. In the second part of the experiment, the dependence of the peak position and FWHM, as well as the changing of the peak shape will be studied as a function of the high voltage applied to the detector, and as a function of the counting rate.

At the recommended high voltage setting, and at a counting rate of about 1000/s determine the position of the Co-60 peaks, and the Cs-137 peak. Perform the energy calibration and determine the resolution; resolution is the FWHM of the 1332 keV peak (the second peak of Co-60), expressed in keV. Also record the peak position and the FWHM of the Cs-137 peak. Observe also the shape of the peaks. If a printer is available, print/plot the spectrum in the expanded mode, so that the second Co-60 peak can be seen clearly. Determine the FWTM (full width at 1/10 the maximum height). If the peak has a true Gaussian shape, the ratio of the FWTM to FWHM will be equal to 1.823. Measured values of 1.90 are good. Larger values indicate that either the charge collection in the detector is inefficient or the counting rate is too high for the system depending on whether the asymmetry is on the low or high energy side of the peak, respectively.

Decrease the high voltage in steps of 500 V; at each setting determine the position (in channels) and the resolution (in keV) of the Co-60 and Cs-137 peaks. Also determine the ratio of the FWTM to FWHM for the 1332 keV Co-60 peak.

Table 5.3.1. Properties of selected calibration radioactive isotopes.

Radioactive isotope	Half life	Gamma ray energies	Emission probability
Co-60	5.2719 y	1173.238	99.89
		1332.502	99.983
Cs-137	30.25 y	661.666	85.20
Mixed source: Co-60, Cs-137 and			
Cd-109	462.6 d	88.034	3.65
Co-57	271.79 d	122.061	85.68
Hg-203	46.6 d	297.179	81.56
Y-88	106.63 d	898.042	94.1
		1836.063	99.36
		2734.086	0.61

Plot the FWHM and peak position as a function of high voltage. Compare the shape of the peaks at the different values of the high voltage.

With a counter, connected to the CRM (counter ratemeter) output of the amplifier, set the counting rate at different values: 100, 1000, 5000, 10000, 40000 counts/s.

At each counting rate, determine the FWHM for different values of shaping time constant (0.5, 1, 3, 6 ms). Plot the family of curves, showing the FWHM/shaping constant (or time constant t). Determine the best shaping constant for each counting rate.

Experiment 2

Using a mixed radioactive source, record a spectrum with good statistics (the main peaks should have at least 10000 counts in the net area). Assuming that the detector is most sensitive at the energy of 120keV, and that the relative efficiency at this energy is 1, estimate the efficiency of the detector at other energies. Plot a rough curve of efficiency as function of energy. For orientation, see Fig. 5.3.4, showing an accurately measured efficiency curve for the detector.

Experiment 3

With the pulser set at a high counting rate somewhere around 50000 counts/s, and using the unipolar output of the amplifier, take the spectrum in such a way that the peak will be in the middle of the screen. Change to the gated integrator output, and take the spectrum again. If possible, print or plot these spectra.

Connect the UNI INH output on the rear panel of the amplifier to the gate of the MCA, and take the spectrum again, using the unipolar signal from the amplifier. Observe the change in the spectrum. Repeat the same with the signal taken from the GI output, and with the MCA gate connected to the GI INH output signal on the rear panel. Try to find an

explanation for the shape of these spectra; probably you will have to carefully observe the signals from the UNI and GI output simultaneously, using a double pulse generator, and changing the time distance between two pulses.

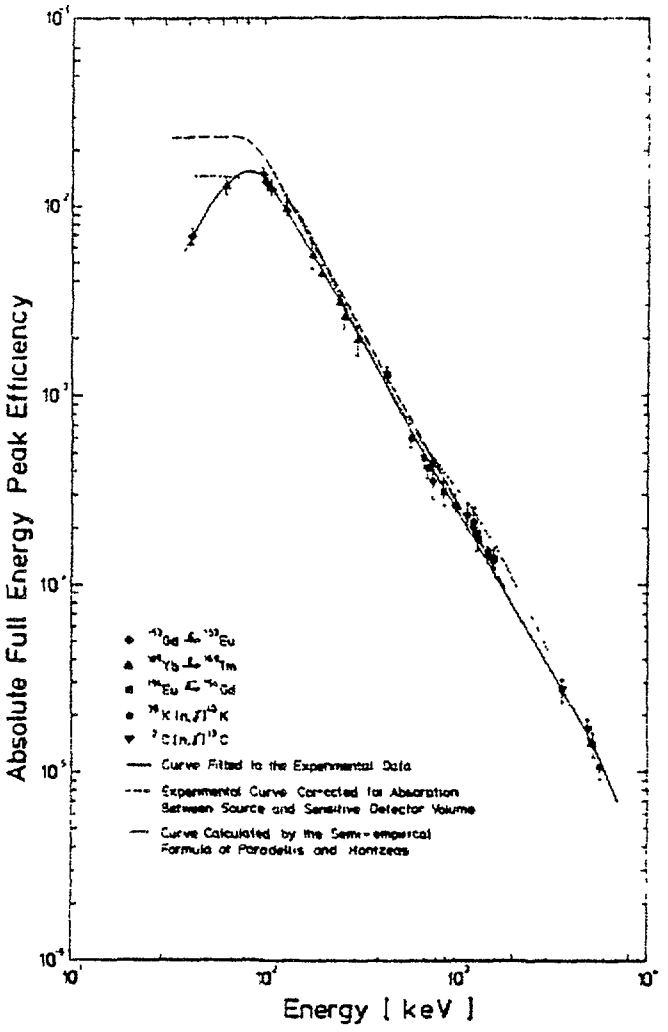


Fig. 5.3.4:

Efficiency curve of a Ge detector.

Notes:

Experiment 5.4

HIGH RESOLUTION X-RAY DETECTORS

OBJECTIVES

The performance and characteristics of Si(Li) and planar Ge detectors will be investigated. The important properties, such as the resolution, pulse shape, and efficiency of the detector will be studies. The behavior of the electronics system for high resolution x-ray spectrometry will be analyzed.

REVIEW

Lithium drifted silicon detectors, planar pure germanium detectors, and occasionally intrinsic (pure) silicon detectors are used in energy dispersive, high resolution x-ray spectrometry. There are some notable differences between Ge and Si detectors for x-ray spectroscopy.

The Si(Li) detector is the workhorse of X-ray analysis. A single crystal of silicon, some 6 mm in diameter and 3 mm thick, with the impurities compensated by lithium atoms, is the detector. Suitable contacts are applied to the surfaces. A bias voltage between 400 and 800 volts is applied. The charges produced by X-rays (the X-ray interacts primarily by the photoelectric process, producing an energetic electron that then loses its energy by ionizing/exciting the silicon atoms) are collected and amplified by a charge sensitive preamplifier.

Most of the manufacturers of the Si(Li) detectors use the optical feedback type of preamplifier. The typical shape of the signals coming from such preamplifier, is shown in Fig. 5.4.1. A simplified circuit diagram of such preamplifier is presented in Fig.5.4.2. Whenever the capacitor C is discharged, the voltage returns to base level in a short pulse. In this preamplifier, as in most high resolution systems, the input FET is located inside the cryostat, and is cooled to reduce the noise level. The charge pulse from the detector is integrated by the feedback capacitor of the preamplifier. Unlike most integrating amplifiers that use a passive resistor in parallel with the feedback capacitor to discharge it, this preamplifier has no resistor, and allows the voltage to build up in a random staircase signal, as shown in Fig. 5.4.1. Periodically, the integrating capacitor is discharged by a pulse of light on drain gate of the input FET, as shown in Fig. 5.4.2. The reset period may be several microseconds long and produces a large negative pulse on the output of the preamplifier.

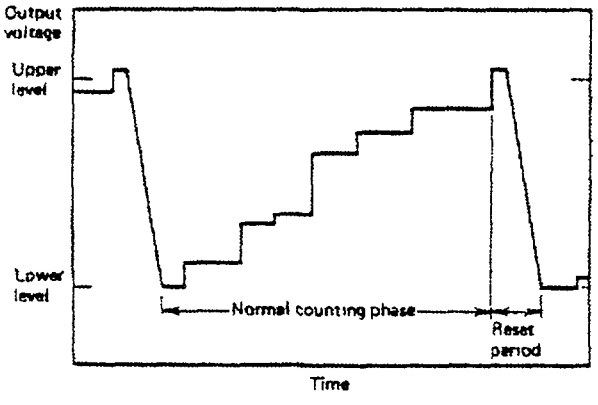
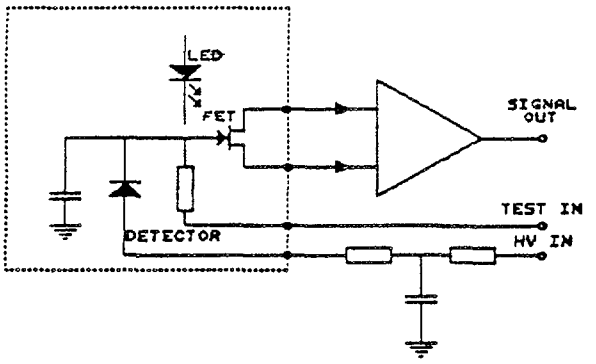


Fig. 5.4.1: Signal from an optical feedback preamplifier.

Fig. 5.4.2:

Shematic of optical feedback preamplifier.

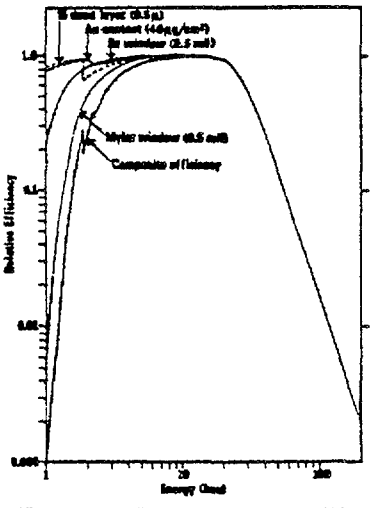


The spectroscopy amplifier for Si(Li) X-ray systems should have the capability of processing the signals with relatively long shaping times (between 6 and 16 ms; most of the manufacturers recommend 12 ms). The discharge of the preamplifier capacitor produces a very large, negative, saturated pulse in the amplifier. This inconvenient signal is eliminated from further processing by an inhibit signal, coming from the preamplifier, and connected to either the gate of the ADC or the amplifier INH input.

The resolution of a Si(Li) detector is defined as FWHM of the Mn-55 K-a X-ray line, at 5.9 keV. An average detector has resolution of 195 eV, and excellent one 165 eV. The intrinsic efficiency of Si(Li) detector is a function of energy. At 10 keV, such a detector is 100% efficient, a typical measured efficiency curve is presented in Fig. 5.4.3.

Fig. 5.4.3:

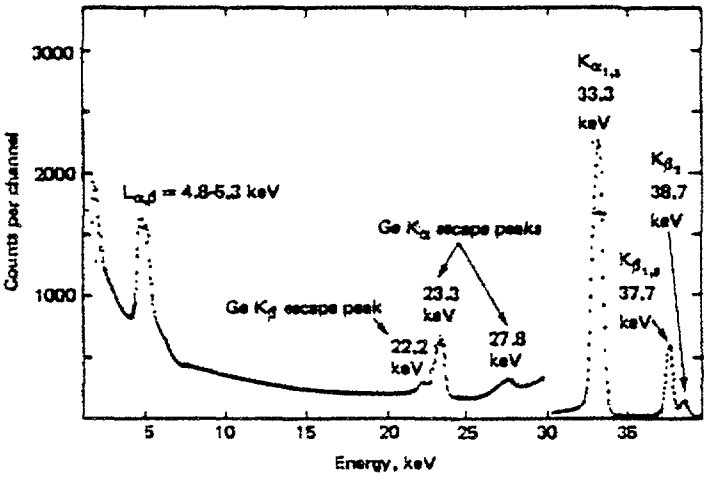
Typical efficiency curve of a Si(Li) detector.



The planar germanium detector stops X-rays more efficiently than silicon. It is better suited to detecting X-rays at higher energies, its range can extend to 200 or 300 keV. If the Ge detector is not as frequently used for X-ray analysis, it is because of the inconvenience caused by the escape peaks. A spectrum of Ce-139 with the escape peak displayed, is in Fig.5.4.4.

Fig. 5.4.4:

Escape peaks in a Ce-139 spectrum.



Experimental setup.

The diagram of the experimental set up is shown in Fig.5.4.5. Note that a precision pulse generator will be used to inject the pulses in the test input of the preamplifier. A counter will be connected to the ICR output at the back of the main amplifier (Canberra 2020/2024); the ICR output provides a TTL logic signal corresponding to the incoming count rate. An oscilloscope is essential for proper adjustment of the spectrometer.

EXPERIMENT

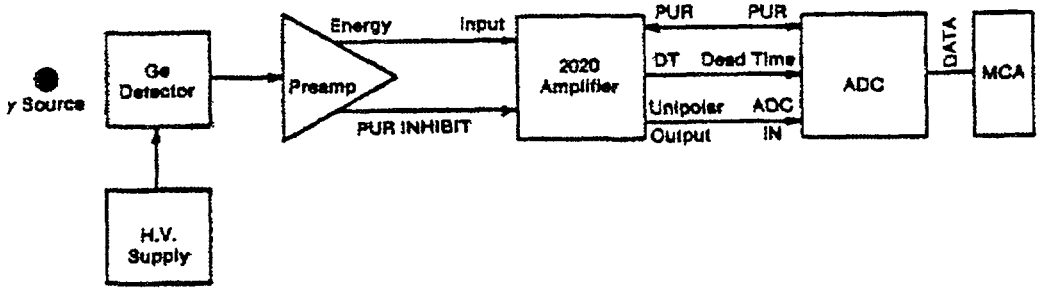


Fig. 5.4.5: Si(Li) system.

From the amplifier, the signal travels to the ADC. This is an NIM module (Canberra 7045), connected to an add-on card (Canberra S100) located inside a PC computer. A printer will be useful to print the spectra. The S100 MCA operates in an environment called WINDOWS. Become familiar with the basic concepts of WINDOWS and S100 operation; use the computer mouse.

Note: Store and save the spectra acquired in experiments 1, 2, and 3 for use in Experiment 4.

Experiment 1: Si(Li) detector properties.

Set the high voltage of the detector as recommended in the certificate. With the oscilloscope, check that the signals from the output of the main amplifier are prroperly shaped. Select the shaping time constant as recommended by the manufacturer.

Adjust Fe-55 radioactive calibration source at such a distance from the top of the detector that the counting rate will be about 1000 counts/s. Check this with the counter.

Take a spectrum of the Fe-55 source. Calibrate it. The calibration is possible with the two peaks of Fe-55, at 5.9 and 6.4 keV, but a better calibration will be achieved if the two calibration peaks are wider apart. A Cd-109 source can be used for more peaks (22.1 and 25.0 keV).

Use both the manual procedure and the built-in computer features to accurately determine the FWHM of the Fe-55 peak at 5.9 keV. This is the resolution value for the detector; compare with the certificate.

Move the Fe-55 source closer to the detector, so that the counting rate will increase to 5000 counts, and determine the resolution. Repeat with the counting rates of 10000, 20000, 40000 counts. Plot the value of the resolution as a function of the counting rate.

Experiment 2: Optimizing the operation of Si(Li) spectrometer

With the oscilloscope, observe the inhibit pulse from the preamplifier in one channel and the amplifier pulses in the other. Compare the duration of the inhibit pulse with the large negative pulse from the amplifier output. The length of the inhibit pulse can be adjusted with a trimmer on the preamplifier. Select the length to be at least four times longer than the amplifier inhibit pulse. Connect the inhibit pulse to the INHIBIT IN connector at the rear of the amplifier. Connect the PUR cable with the corresponding connector on the ADC. Connect the DT output at the rear panel of the amplifier with the gate input in the ADC. These connections will ensure that the dead time corrections of the ADC will be performed properly.

Take a spectrum of a Cd-109 source at a high counting rate, say 40,000 counts/s; simultaneously count the incoming signals with the counter connected to the ICR output of the amplifier. Set the live time on the MCA and the time on the counter both for 100 seconds. Compare the total number of counts accumulated in the MCA in live time mode, with the number of counts collected by the counter in the real time mode. If the dead time corrections are correctly implemented, they should be the same.

Take a spectrum of a Fe-55 source at high counting rate twice, first with the pileup rejector off and then with pileup rejector activated. Compare the spectra quantitatively, i.e. determine the ratio of the full energy peak to the total counts in the spectrum above the peak, for both cases, and compare them.

Shorten the width of the inhibit pulse from the preamplifier by adjusting the trimmer, to a value equal to the width of the negative inhibit pulse from the amplifier. Take the spectrum, and explain the strange tail on the low energy side of the full energy peak.

Experiment 3: Planar Ge detector.

Adjust the bias voltage of the detector to the value recommended by the manufacturer. Optimize the operation of the planar Ge detector by adjusting spectroscopy amplifier settings and take a spectrum of Fe-55. Use a counting rate of about 5000 counts / second. In this case the preamplifier does not have an optical feedback system so the setup will be easier but the performance of the system will probably not be as good. Take a spectrum of Fe-55, perform the energy calibration, and determine the resolution of the 5.9 keV peak.

Take a long measurement with the Cd-109 source, so that you will have at least 100,000 counts in the Cd-109 K-a full energy peak. Determine the area accurately, using the build-in algorithms of the MCA card. Identify the escape peak, and determine its area. Determine the ratio of these areas, and compare with the theoretical value. Why did you not observe a similar escape peak in the Fe-55 spectrum?

Experiment 4: X-ray spectrum analysis.

Install in the computer the QXAS (quantitative X-ray analysis system) software, and analyze the spectra accumulated in the previous experiments with the help of AXIL analysis programme. (The QXAS manual is available separately). Compare the results of the FWHM and area determinations with the ones made by hand or by the emulation software of the S100 MCA card.

EXPERIMENT 5.5

NEUTRON DETECTION

OBJECTIVE

This experiment will demonstrate one type of pulse neutron detector as well as demonstrate some of the properties of proportional detectors.

REVIEW

Radiation detectors operate by detecting the ionization or excitation of the atomic electrons by radiation. Neutrons do not interact with electrons and, therefore, can not ionize or excite atoms. Neutrons interact only with the nucleus of atoms. In addition, it takes energy, a minimum of a few eV, to produce ionization or excitation of atoms and frequently the energy of neutrons are measured in millielectron volts (0.001 eV). Thus, many neutrons do not have enough energy to be detected. In order to detect neutrons, one must incorporate a nuclear reaction in the detector that will produce some type of ionizing radiation (protons, alpha particles, energetic electrons, or gamma rays) that can be detected. In addition, these nuclear reactions may also have to be exoergic (more kinetic energy out of the reaction than goes into the reaction) in order to supply the energy for the detection process.

Nuclear reactions that are commonly incorporated into radiations detector are:

$$^{10}B + n \rightarrow {}^{7}Li^{*} + \alpha + 2.310 \text{ MeV}$$
$$^{6}Li + n \rightarrow {}^{3}H + \alpha + 4.78 \text{ MeV}$$
$$^{3}He + n \rightarrow {}^{3}H + p + 0.765 \text{ MeV}$$
$$^{235}U + n \rightarrow \text{fission} + 160 \text{ MeV}$$

The B-10 and He-3 reactions are frequently used in gas detectors (ionization or proportional detectors). The boron may be a coating on the detector walls or added as BF_3, a good proportional counter gas. Helium-3 is a good counter gas. Lithium-6 occurs naturally in lithium or may be enriched. The lithium is usually incorporated in detectors as LiI(Tl) scintillation detectors. The fission process is usually used by coating the walls of ionization detectors with U-235.

In order for a nuclear reaction to be useful in the process of detecting neutrons, it must also have a high probability for neutron interactions. The four reactions listed above all have interaction probabilities or cross sections that vary inversely with the neutron velocity. Thus, the less energy the neutron has, the higher the probability that the neutron will be detected. Most neutrons are "born" or produced with high energies. The average energy for neutrons coming from the fission process is 2 MeV. On the other hand, for neutrons to be detected efficiently, they should have energies less than 1 eV. To slow the neutrons down so they can be detected, the neutron detectors are frequently placed inside of shields containing hydrogen (paraffin - plastic - water). The neutrons hit the protons (the nucleus of the hydrogen atom) and give up part of their kinetic energy. After repeated

collisions with hydrogen (between 10 and 14) the neutron energy will be less than 1 eV and the neutron can be readily captured by the neutron detector. Note that in this mode of operation, the detector is only counting the number of neutrons and gives no information concerning the energy of the neutrons.

Most neutron detectors are also relatively efficient gamma-ray detectors and gamma rays are always present with neutrons. Therefore, it is desirable to be able distinguish between neutron and gamma-ray events in the detector. Fortunately, in the gas detectors, the gamma-ray detection process usually allows only a small fraction of the gamma-ray's energy to be deposited in the detector and simple pulse height analysis (the pulse height is proportional to the energy deposited in the detector) can be used to separate the neutron events from the gamma rays. In some cases, more elaborate technique such as analyzing the rise time of the detector pulses are used to distinguish between the neutron and gamma-ray events.

Experimental setup

EXPERIMENT

For this experiment a small BF_3 detector will be used. The detector will operate as a proportional counter with BF_3 as the counting gas. Placing the boron in the gas is an advantage because both the Li-7 and the alpha particle (both are ionizing particles and share the reaction energy) are in the gas, producing ionization. If the boron is on the walls of the detector, then only one of the two particles, either the Li-7 or the alpha particle enters the gas, producing ionization. In this case, the maximum energy that can be deposited in the detector is 1.47 MeV rather than 2.31 MeV making the separation of neutron and gamma-ray events more difficult.

Most systems using BF_3 detectors use only a simple integral single channel analyzer (SCA) following the main amplifier. The output of the SCA is used to drive a scaler-timer. This arrangement allows discrimination against the gamma rays. In this experiment, we will use a multichannel analyzer (MCA) to look at the spectrum of pulses from the detector and then use a region-of-interest (ROI)to represent an integral discriminator and scaler-timer.

WARNINGS

The neutron source must be handled with care. Neutrons are probably the most dangerous type of nuclear radiation because of their energy and relative biological effect. In addition, neutron sources also are sources of gamma rays. For every neutron produced, when the neutron is finally absorbed in a nucleus (a few milliseconds after it is produced) between 1 and 10 gamma rays will be emitted with an average energy of about 1 MeV. Therefore, do not stand near the exposed source and use a long cable (3 to 4 meters) between the detector and the preamplifier and the electronics.

The diagram of the electronics system for this experiment is shown in Fig. 5.5.1.

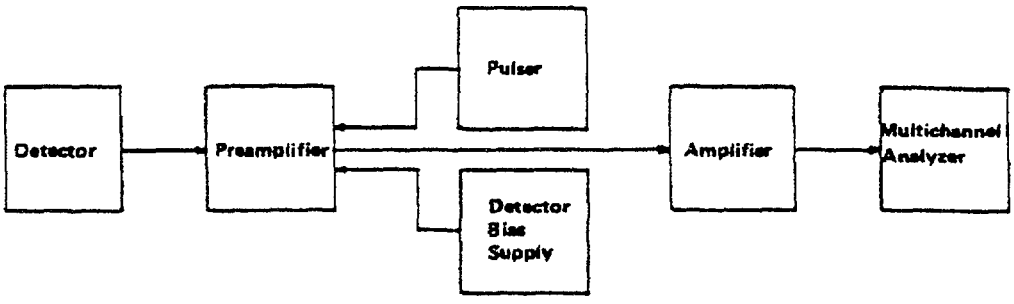


Fig. 5.5.1: Neutron counting system.

Experiment 1

Connect the system as shown in Fig. 5.5.1.

(i) Place the detector in the neutron shield container. The counting rate will probably be very high, so the detector will probably have to be partially withdrawn to adjust the counting rate to about 2000 counts per minute. Set the bias voltage to the value recommended by the manufacturer. Adjust the gain of the amplifier so that the spectrum of pulses from the detector covers about 60 percent of the range of the MCA. Use a conversion gain of 1024 on the MCA. Record and store a spectrum in the first half or fourth of the MCA memory. The events on the left of the spectrum (the low energy side) will be due to gamma rays interacting in the detector while the events on the right side of the spectrum will be caused by events depositing more energy in the detector (primarily neutron events).

(ii) Remove the detector from the neutron source and move the source at least ten feet away from the detector. Place a strong (high intensity) gamma-ray source near the detector and again record a spectrum from the detector using the second half of the MCA memory. Use the same live time as in part i. Compare the two spectra (use the overlap feature of the MCA).

(iii) Determine a channel, below which mostly gamma-ray events are recorded and above which mostly neutron events are recorded. Use this channel as the lower end of a ROI. Set the upper boundary of the ROI at channel 1000. The MCA and the ROI now represent a very expensive SCA and scaler-timer operating in the integral discriminator mode with the lower edge of the ROI representing the discrimination level.

In simple electronic counting systems, there are usually three controlling variables which must be optimized for the best operation of the system; the bias voltage (may affect the amplification of the detector signal in the detector), the amplifier gain, and the discrimination level. Most procedures call for two of the three variables, usually the amplifier gain and the discrimination level, to be fixed and the third variable, the bias voltage to be adjusted to give the optimum performance. In the next part of this experiment, we will explore this method as well as one where the voltage and gain are predetermined and the discrimination level adjusted.

(iv) Use the amplifier gain determined in part i and the ROI determined in part iii. Place the detector in the neutron shield and adjust the counting rate to about 2000 counts per minute. Lower bias voltage about 150 volts, record a spectrum and determine the number of counts in the ROI. Record the number of counts in the ROI.

(v) Raise the voltage by 25 volts and again accumulate a spectrum and determine the number of counts in the ROI. Note on the MCA how the distribution of pulses changes with respect to the lower limit of the ROI (the discrimination level). Repeat the measurement until the voltage is at about 100 volts above the recommended voltage. Plot the number of counts in the ROI as a function of the bias voltage. This is representative of the normal plateau curve associated with many types of gas detectors and even some scintillation detector applications. On your curve note the point corresponding to the recommended voltage. The number of counts in the ROI may decrease at the highest voltages. Explain why this occurs. Note that a similar plot would be obtained if the voltage were held constant and the amplifier gain changed.

(vi) Return the bias voltage to the recommended voltage and record a spectrum. Change the lower limit of the ROI to channel 10 and record the number of counts in the ROI. On the same spectrum, increase the lower limit of the ROI to 20 and again record the number of counts in the ROI. Repeat, increasing the lower limit of the ROI in steps of 10 channels and plot the number of counts in the ROI and a function of the lower limit. This is representative of the integral discriminator curve. Again note the location of the previously determined optimum point on the curve.

Experiment 2: Neutron detection

(i) Using the recommended bias voltage and the values of the amplifier gain and ROI determined in parts i and iii in the preceding experiment, place the detector in one of the tubes in empty detector can. Place the neutron source in the other tube in the can. **DO NOT TOUCH THE SOURCE WITH YOUR HANDS. DO NOT STAND NEAR THE SOURCE ANY LONGER THAN NECESSARY.** Accumulate a spectrum and record the number of counts in the ROI.

(ii) Fill the detector can with water, being careful not to get any water in the tubes with either the detector or the source. Again accumulate a spectrum for the same live time used in part i and compare the spectrum and the number of counts in the ROI. Explain the results.

(iii) Remove the detector, cover it with a piece of cadmium and replace it in the tube. Again accumulate a spectrum, determine the number of counts in the ROI, and compare with the results in parts i and ii. Explain you results.

(iv) Remove the cadmium from the detector, but cover the source with a thin piece of cadmium. Repeat the measurements and explain the results.

EXPERIMENT 5.6

COINCIDENCE EXPERIMENT

OBJECTIVE

The objectives of this experiment are to explore the timing of nuclear signals. Some of the problems in generating timing signals will be demonstrated as well as the characteristics of a slow coincidence circuit.

REVIEW

In many nuclear applications, the timing of the event or of the detection of the radiations is equally or sometimes more important that knowing just the energy of the radiation. All of the previous experiments have concentrated on the characteristics of various nuclear detectors and on energy spectroscopy. However, many applications require that two or more events be detected simultaneously by two or more detectors. A number of medical diagnostic techniques require that the two 0.511 photons from positron annihilation be detected simultaneously. If the two photons are both detected in two different detectors at the same time, then one can be reasonably assured that the two photons came from the same positron rather than from two separate events just close in time. In this type of experiment, the two annihilation photons are considered to be detected at the same time if their time separation is no more than 10 nanoseconds. Another common application of coincidence counting is found in many liquid scintillation detectors. In most liquid scintillation detectors, the liquid scintillator is observed with two photomultiplier tubes. The outputs of the photomultipliers tubes are added or summed together to give the total pulse. However, because of the low energy usually involved and the poor efficiency for light collection, the photomultiplier tubes must be operated in the noise regions where the dark current from the photocathode contributes significantly to the number of output

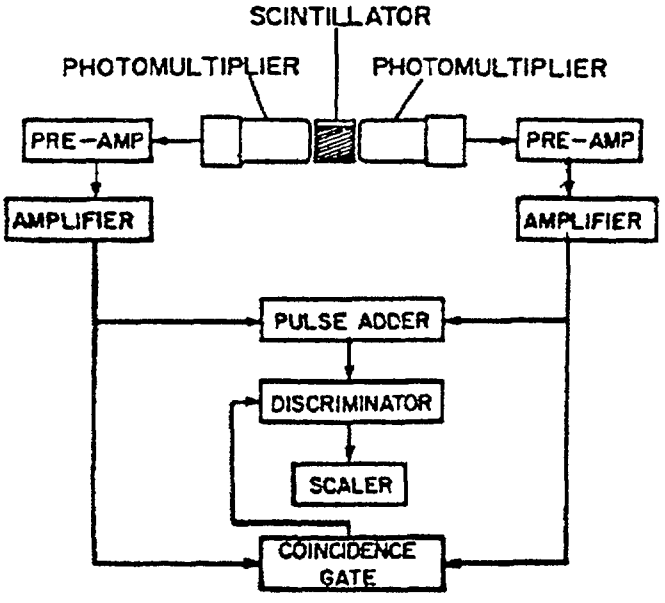


Fig. 5.6.1: Coincidence system for liquid scitillation detector.

pulses. In order to reduce the number of false events, only those events that are recorded by both photomultiplier tubes simultaneously are considered to be true events originating in the liquid scintillator. Therefore, the outputs of the photomultipliers are first sent to coincidence circuit and if the event is true event, then the output of the summing circuit is sent to the pulse height analyzer. See Fig. 5.6.1.

Leading edge timing

The simplest and most straight forward method of generating a timing signal is to send the pulse from the preamplifier or amplifier to a simple discrimination level such as a Schmitt trigger. The output is triggered when the leading edge of the input signal crosses the discrimination level. This method works well if the amplitude of the input pulse is uniform and all of the input pulses have the same rise time. Unfortunately, the output of nuclear detectors are usually random in amplitude and depending on the type of detector, the rise time may vary by a factor of 10. An example of the problems encounter are shown in Figs. 5.6.2 and 5.6.3 for amplitude and rise time variations respectively.

Fig. 5.6.2:

Leading edge timimg with different amplitudes.

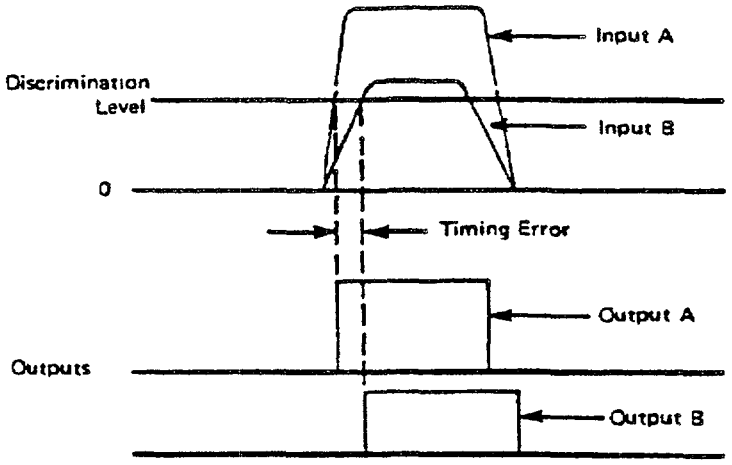
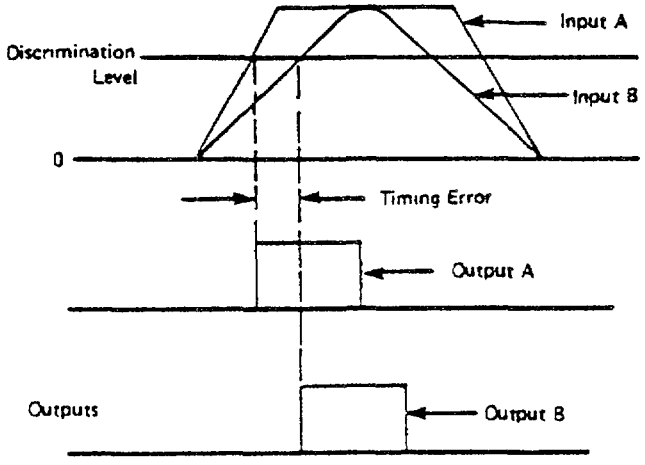


Fig. 5.6.3:

Leading edge timing with different risetimes.



Crossover timing

Some of the problems encountered with leading edge timing can be minimized with crossover timing.

The point at which bipolar output pulses from the amplifiers cross from the positive to the negative lobe remains relatively constant in time. This is true for pulses with varying amplitude. Therefore, if a timing discriminator that senses the crossover point will produce a pulse that is independent of the energy of the event. See Fig. 5.6.4.

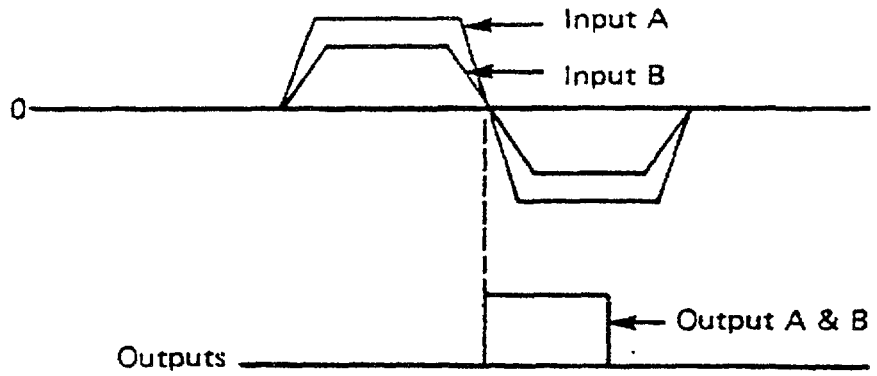


Fig 5.6.4: Crossover timing.

This method will work well for detectors such as NaI(Tl) scintillation detectors and will typically allow timing down to +/- 10 nanoseconds. Unfortunately the crossover point is still a function of the rise time of the detector pulse and, therefore, the technique does not work well with detectors such as large Ge solid state detectors. Variations in the crossover point are frequently used as the basis for systems that measure the rise time or shape of detectors signals.

Constant fraction timing

An improved timing technique, called constant fraction timing (CFT) is shown in Fig. 5.6.5.

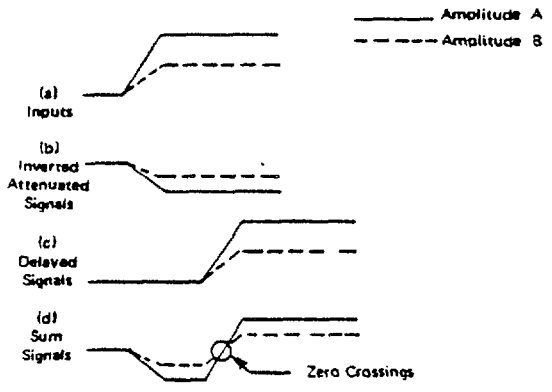


Fig. 5.6.5: Constant fraction timing.

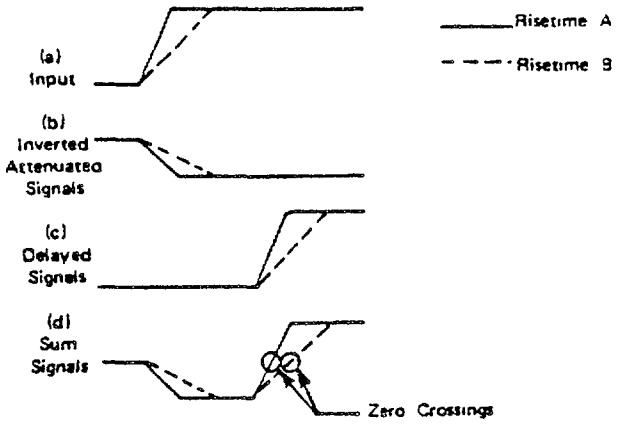
In this technique, the input signal is divided and one part of the signal is inverted and attenuated and then summed with the delayed (uninverted and unattenuated) signal. This produces a signal with a zero crossing as shown in Fig. 5.6.5. This method works well for both unipolar and bipolar pulses with varying amplitudes, but still does not compensate

for variations in detector rise time. See Fig. 5.6.6 However, by using short delay times on the unattenuated portion of the signal (delay times equal to or shorter than the minimum rise time expected from the detector), time resolutions as short as 10 nanoseconds can be achieved with large Ge detectors over a reasonable energy range.

This experiment will be done in two parts. The first part will demonstrate some of the problems encountered with leading edge time and the stability of constant fraction timing with changes of amplitude. The second part of the experiment will use two scintillation detectors to investigate a few of the properties of annihilation radiation and coincidence counting.

Fig. 5.6.6:

Constant fraction timing with different risetimes.



Experiment 1

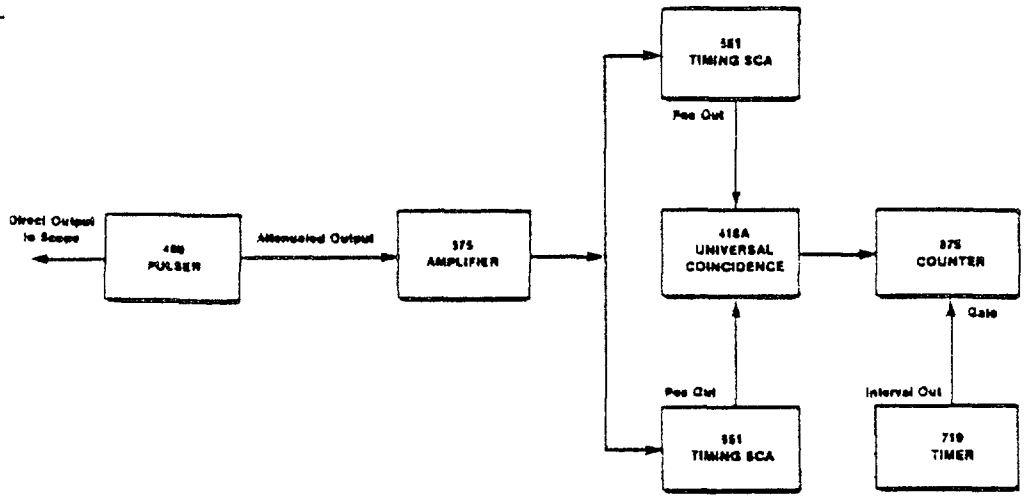
EXPERIMENT

Connect the equipment as shown in Fig. 5.6.7.

Connect the attenuated output from the pulser to the input of the amplifier. With all of the attenuating switches off, adjust the gain of the amplifier and the pulse amplitude from the pulser to yield an amplifier output pulse about 8 volts high. Connect the direct output

Fig. 5.6.7:

Equipment diagram for Experiment 1



from the pulser to the external, delayed trigger of the oscilloscope. Set the lower level discriminator (LLD) on the SCA to 0.5 volts. (The input range of the SCA is 0 to 10 volts and the LLD is a ten turn control with 100 divisions per turn. Thus the LLD can be controlled to 1 part in 1000.)

(i) Use the oscilloscope to measure the rise time of the pulses from the amplifier.

(ii) Using the external delayed trigger on the scope, trigger the scope with the direct output from the pulser. Connect the LLD output from one of the SCA's to one of the vertical inputs to the scope; measure and record the pulse amplitude, width, and delay time from start of the scope trigger signal. The LLD output signal from the SCA is triggered by the input pulse crossing the discrimination level and is an example of simple leading edge timing.

(iii) Using the attenuator switches on the pulser, reduce the amplifier output by a factor of 2 (4 volts). You should not have to make any adjustments to the scope trigger, since the scope is being triggered by the direct, unattenuated signal from the pulser. Again measure and record the delay time between the scope trigger signal and the LLD output. Repeat with attenuation factors of 5 (1.6 volt output) and 10 (0.8 volt output). Determine the change in the timing of the LLD signal between the unattenuated signal and the X 10 attenuated signal and compare to the rise time of the amplifier pulse. Plot the change in the delay time as a function of the amplifier pulse amplitude.

(iv) Repeat the experiment performed in parts ii and iii but use the SCA output. Adjust the delay control on the SCA to its minimum value. The SCA output uses a variation of the constant fraction timing that corresponds to triggering the SCA output when the trailing edge of the amplifier pulses falls to 50 % of the peak amplitude. Verify this by looking at amplifier output on one input of the scope and the output of the SCA on the second input. (You will probably have to use the alternate sweep mode rather than the chopped sweep mode on the scope) In order to make accurate measurements of the time, you can delay the scope trigger and expand the time sweep of the scope to 0.1 microseconds / cm. Again plot the change in the delay time as a function of the amplifier pulse amplitude. Compare your results with the plot of part (iii).

(v) Triggering the delayed trigger of the scope with the direct output from the pulser, look at the SCA outputs of the two SCA's (SCA1 and SCA2). Set the delay on SCA1 to the minimum value and the delay on SCA2 at 3 microseconds. Set the sweep speed of the scope to 0.5 microseconds. Adjust the trigger delay on the scope so that the signal from SCA1 is on the left edge of the scope. Observe the time separation between the two SCA pulses. Connect the two SCA outputs to inputs B and C of the coincidence module. Set the coincidence requirements to 2 and connect a counter to the output of the coincidence module. Turn the counter (scaler) on. Make a logic table and check to see if the counter is counting under the following three conditions.

a) Inputs B and C both in coincidence mode.

b) Input B anti-coincidence and input C coincidence.

c) Input B coincidence and input C anti-coincidence.

(vi) Set inputs B and C on the coincidence module both to coincidence and increase the delay on SCA1 to 1 microsecond. Observe the relative pulse times on the scope and record the counting rate of the counter. Repeat, increasing the delay on SCA1 in steps of 0.1 microseconds until the total delay is 6 microseconds. Plot the counting rate as a

function of the delay. The width of the plot is the resolving time of the coincidence circuit and should be the sum of t1 and t2 where t1 and t2 are the widths of the SCA outputs for SCA1 and SCA2 respectively. The normal operating condition would be with the delay of SCA1 set in the middle of the peak.

(vii) Input A on the coincidence module has an internal trigger that will generate a pulse that can be varied from 0.1 to 2 microseconds independent of the width of the input pulse. Put the SCA signal from SCA1 into input A of the coincidence module and adjust the width of the pulse to 1.5 microseconds. (A test point for inspecting the pulse is provided on the front of the coincidence module.) Repeat experiment v. What is the resolving time of the coincidence module under these conditions?

Experiment 2

Connect the equipment as shown in Fig. 5.6.8.

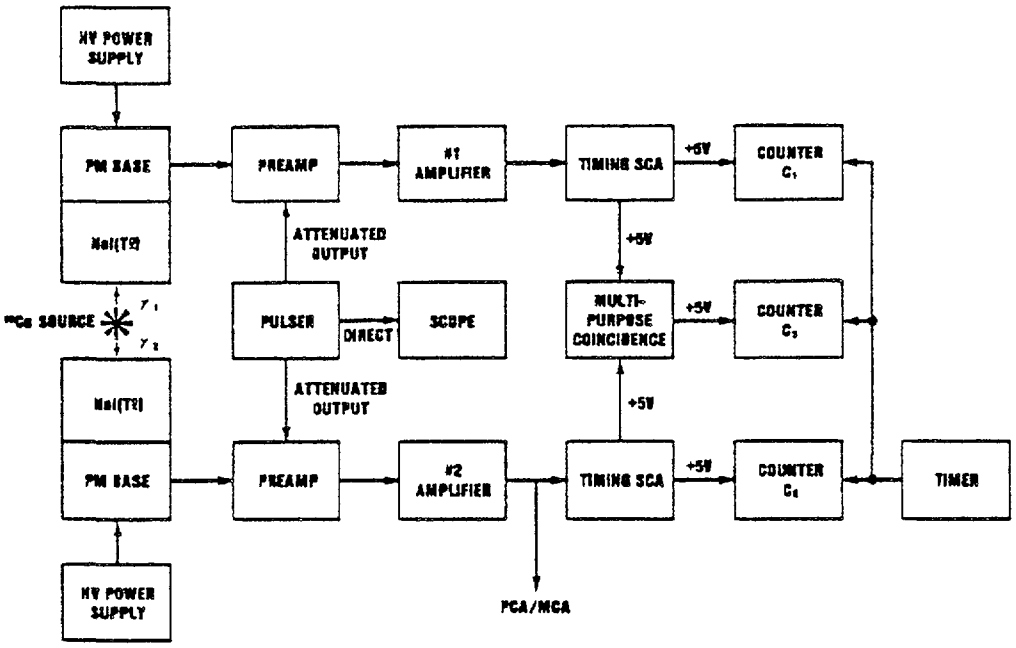


Fig. 5.6.8: Equipment diagram for Experiment 2.

The timer should be connected to control the timing on all three counters at the same time. The MCA and pulser will be used to quickly set the upper and lower level discriminators (ULD and LLD respectively) of the SCA's to the desired energies. The high voltage supply has two outputs, so both scintillation detectors will have the same bias voltage and the gain of each system will be have to be controlled by the gain of the amplifiers.

Sodium-22 decays by emitting a positron (positive electron) followed almost immediately by a 1.275 MeV gamma ray. The positrons will interact in the source within a few nanoseconds, annihilating with an electron, producing two 0.511 MeV annihilation photons. The 1.275 MeV gamma ray also appears within a few nanoseconds after the original decay of the Na-22 nucleus and, therefore, both annihilation and the 1.275 MeV gamma ray can be considered to be in coincidence for our system. A typical pulse height spectrum for NaI(Tl) scintillation detectors is shown in Fig. 5.6.9.

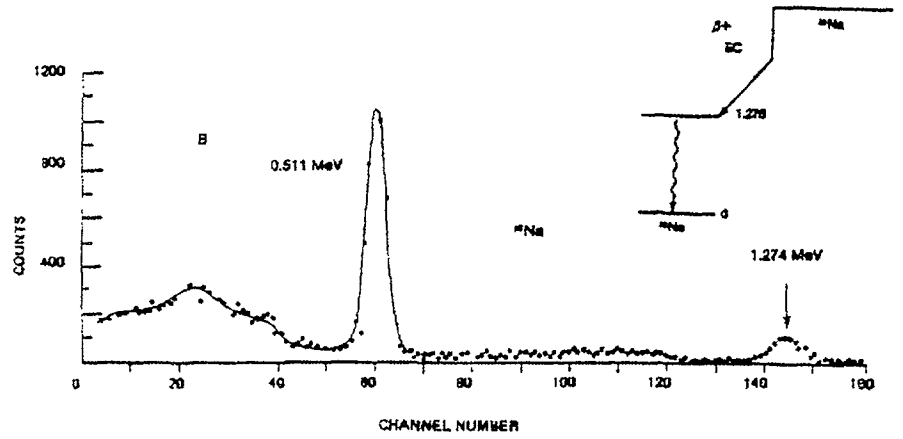


Fig. 5.6.9: Na-22 spectrum.

Set the bias voltage to about 950 volts and using a "T" connector, connect the output of the amplifier to both the SCA and the MCA. Using a Na-22 source, acquire a spectrum on the MCA, adjusting the gain of the amplifier so that the 1.275 peak falls in the region around channel 800 on the MCA. (Use 1024 conversion gain on the MCA.) Determine a ROI to include the 0.511 MeV peak and connecting the pulser to the test input of the preamplifier, set the pulser to give a peak at the lower limit (LL) of the ROI. Now with the SCA set in the normal mode, (the LLD and ULD controls operate independently to allow one to set a wide window for the SCA output.) and starting with the LLD at 0 and the ULD at 1000 and the counter on, adjust the LLD until the counter stops counting. The setting of the LLD now corresponds to the LL of the ROI. Now adjust the pulser to give a peak at the upper limit UL of the ROI and adjust the ULD of the SCA until the counter again stops counting. The window of the SCA is now adjusted to count only events falling in the 0.511 MeV peak of the spectrum. Check by moving the pulser to the center of the peak and check to see if the counter is counting.

Repeat the procedure for the second scintillation detector and system.

Adjust the delays of the SCA to provide coincidence pulses as determined in part v of Experiment 1. This should complete the calibration and setup of the equipment. Both detectors will be counting only 0.511 MeV photons from the annihilation process. Explain why this is really not a true statement.

Now tape each detector to a meter stick so that the face of the detector is 15 cm from the end of the meter stick.

(i) Using a sealed Na-22 source, place the two detectors in a straight line, each 16 cm from the source. Using the timer to control all three counters, measure the counting rate of system 1 (N1), system 2 (N2), and the coincidence circuit (N_{cc}). The counting time may have to be fairly long in order to get a meaningful number of counts in the coincidence circuit.

(ii) Now move the detectors so they are 90 degrees to each other but still at a distance of 16 cm from the source. Using the same time as in part i, repeat the counting and compare the three sets of counts. N1 and N2 in each case should be about the same if the source to detector distances were kept the same. Explain the differences in the two values of N_{cc}.

(iii) Re-calibrate one of the two detector systems so that the SCA window is covering the 1.275 MeV peak. and repeat experiments i and ii. Explain the differences in the results.

(iv) Change the delay on one of the SCA's by 3 microseconds and take a measurement. In this case, there should be no true coincidences and the number of counts in N_{cc} represent the accidental coincidences. The number of accidental coincidences will of course depend on the counting rate. The higher the counting rate, the greater the probability that two separate events will interact in the two detectors at the same time. The number of accidental coincidences also varies inversely with the coincidence resolving time. The shorter the resolving time, the smaller the probability that two accidental events will be counted as a true event. The number of coincidences should always be corrected for the number of accidental events. There may also be true events in the background and these should also be measured and corrections made for them.

Concluding Comments

In Experiment 2, part (i) where the two 0.511 photons from one annihilation were detected as a coincidence event, we know only that the event took place somewhere on a straight line between the two detectors since the two photons emerge from the annihilation at an angle of 180 degrees from each other.

With this system, it is not possible to determine the distance from the source to either detector. If a fast timing system were available, the time difference between the two systems could be used to determine the relative distance between the source and the midpoint between the two detectors since the photons travel at a speed of 30 cm per nanosecond. Very good timing systems can measure time differences as small as one picosecond. Using slow coincidence systems such as was used in this experiment, the location and distribution of the source can be examined by revolving the counting systems around the source region.

PART SIX

SPECIAL PROJECTS

Special projects - an introduction.

The IAEA central annual training course on nuclear electronics features one specific approach which has found enthusiastic acceptance by the participants. Each student selects, during the first weeks of the course, a specific problem. By the end of the course, the participant is expected to solve it. The selected topic can be the design and construction of a nuclear electronic unit, the evaluation of a commercial instrument, or the development of computer software. The technical level, and the nature of these "special projects" varies in a wide range: from a simple radiation monitoring device, to a multichannel analyzer, from a three-transistors unit to a printed board including programmable integrated circuits.

In Part Six of the Nuclear Electronics Laboratory Manual, ten special projects are presented. They have been selected from among the more successful projects of the past three years, and cover all the topics elaborated in the previous parts of the Manual.

The first project, a power supply for modular units in EUROcard system, is described in great detail: in the IAEA training course, each participant has to construct this instrument, becoming closely familiar with a modern design of such a unit that incorporates a number of features not found in the traditional NIM power supply. The most demanding project in the manual is a complete multichannel analyzer, described in two special projects.

The use of personal computers in nuclear experiments is receiving increasing attention. Nowadays it is hard to imagine the design of printed boards, and study of circuits without help from computers. Tribute to this development is paid by the last two experiments in the Manual.

Special project 6.1

EURO BIN AND POWER SUPPLY

To assemble and test the power supply for applications in nuclear instrumentation.

OBJECTIVE

GENERAL DESCRIPTION

REVIEW

This instrument consists of a bin and a low voltage power supply. Four output voltages (+5V; +24V; ±15V) are provided to supply plug-in units of an IAEA Eurocard nuclear measuring system. The voltages are stabilized with integrated power regulators, which are mounted on heat sinks at the rear side of the crate. Other components of the power supply are mounted on a printed circuit board (PCB). The different output voltages have separate power return lines to avoid interactions caused by the return currents.

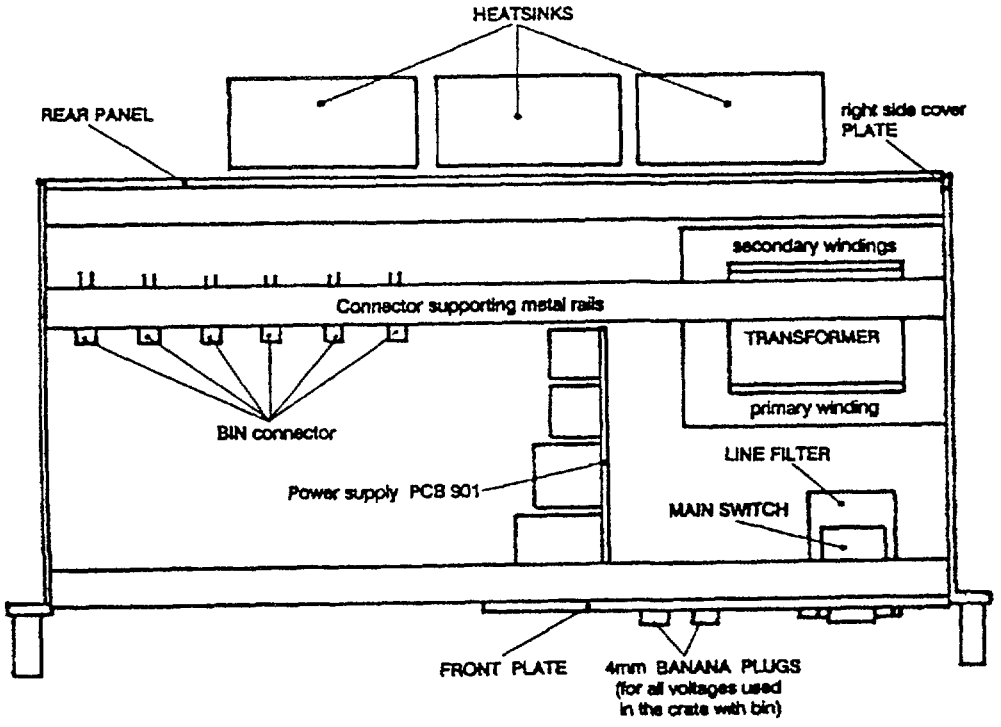


Fig 6.1.1:

Bin with power supply (top cover removed).

SPECIFICATIONS

AC - INPUT

Nominal voltages	110/220V +15 or - 15V selectable)
Rated voltages variations	+10% to -25%
Frequency	47 Hz - 64 Hz
Thermal protection	The transformer is protected by a thermal cutout-switch; "OFF" at 105°C winding temperature, "ON" again at 100° C.

DC - OUTPUTS

	+5V	+/-15V	+24V
Max current	2.5A	1A	1A
Temp. coefficient (1)	0.01%/°C	0.5%/°C	0.05%/°C
Regulation (2)	+0.75%	+0.075%	+0.75%
Ripple and noise	all 1.5mV rms		
Thermal protection	The power regulators are protected thermally by temperature dependent current fold-back circuitry. All outputs are short circuit proof.		

(1) over a range 0°C to 45°C

(2) over the combined range of zero to full load and rated input voltage variations from +10% to -25% of the nominal values.

(3) maximum ambient temperature 45°C

CIRCUIT DESCRIPTION AND THEORY OF OPERATION

A complete circuit diagram is given in Fig. 6.1.2 on the next page. At first glance, the circuit may appear quite complicated; but it is just four ordinary, but well designed, power supplies.

A line filter at the input, which includes the power plug, suppresses noise from the mains. The power switch has a pilot light which indicates "power on". A varistor (transient suppressor) across the lines between the power switch and the transformer limits the energy of spikes, which might come from the supply line or when the transformer is switched off. A thermo-switch in the primary windings switches off the power when the temperature of the transformer windings exceeds 105°C and switches on again at 100°C.

This is necessary since the transformer has to supply more than one secondary winding and the fuses on the primary side are not able to protect the transformer against overheating if one of them is overloaded. Taps on the primary windings allow line voltages 15 V above or below the nominal voltages of 110V or 220V to be used. The set voltage could be the average value over the workday. The power supply itself is able to regulate input voltage fluctuations between +10% and -25%.

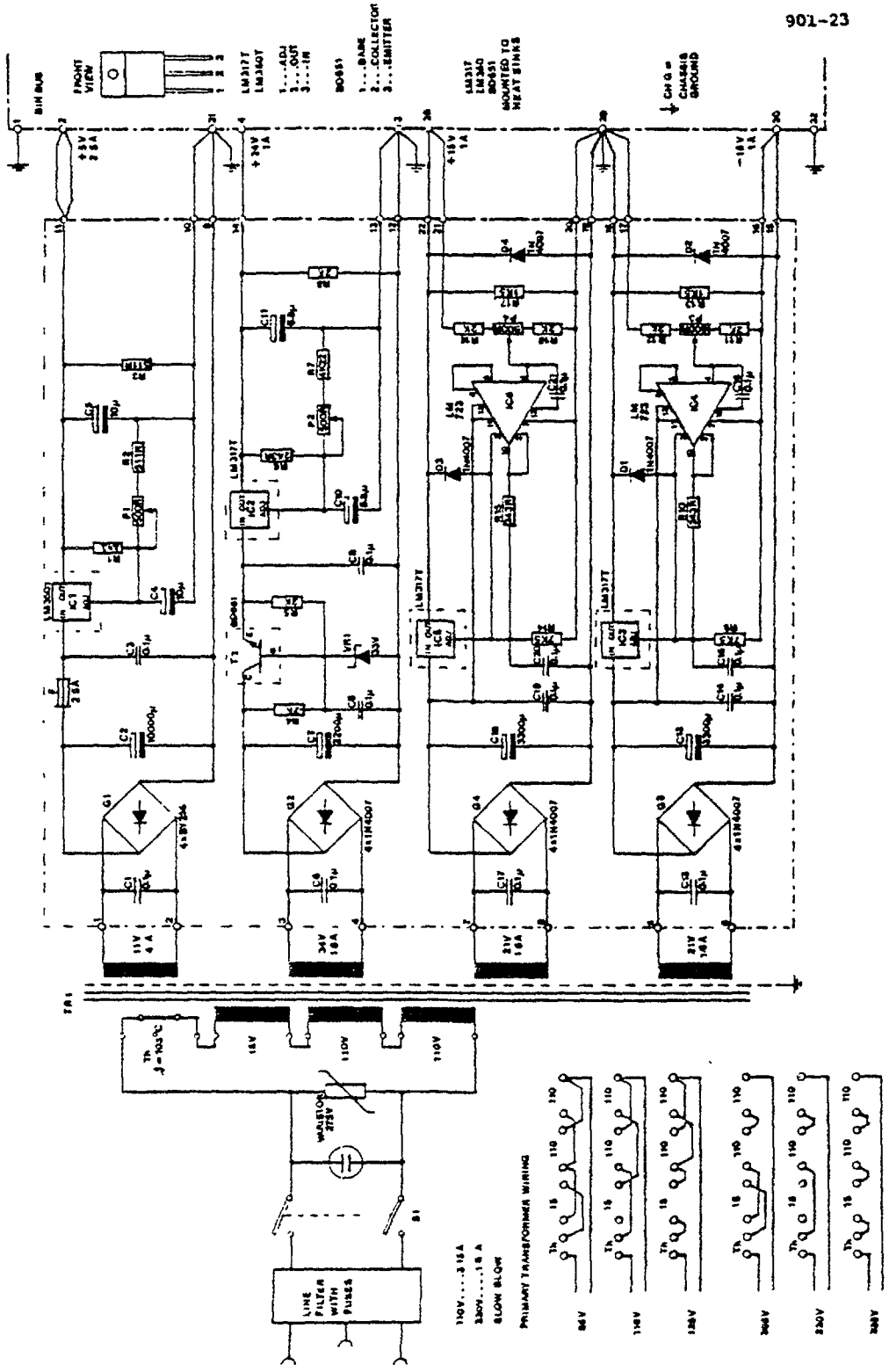


Fig. 6.1.2:

Circuit diagram of the 901 power supply.

There are four windings on the secondary side: 11V, 21V, 21V, and 34V. These low voltage supply sources are connected to the rectifier circuitry on PCB 901. The unregulated DC voltages are connected to inputs of 3-terminal adjustable power regulators (T1 is used as a preregulator), which are mounted on heat sinks at the rear panel. The four regulated DC output voltages are supplied to a power distribution wiring, the bin bus.

Sense lines are used to connect the terminals 10, 13, 16, 17, 20 and 21 (on the PCB) to the bin bus lines 3, 28, 29, 30, and 31. The voltage drops across the sensed supply lines (9-31, 12-3, 22-28, 19-29, 18-29 and 15-30) are compensated by the regulators for the rated supply current ranges; constant nominal voltages are available on the bus. The sense lines and power return lines are joined on the lines 3, 29, 31 of the bin bus. Each of these lines is connected via a separate wire to chassis ground (instrument case) on the side panel.

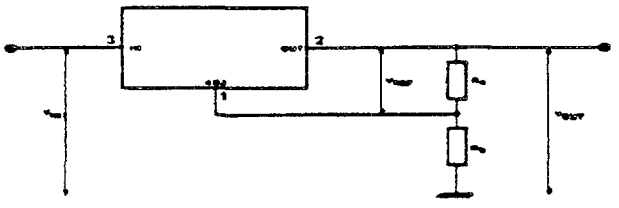
This technique avoids interacting compensation currents. Bin bus lines 1 and 32 are connected also to chassis ground to provide a possibility for grounding the front panels via the PCBs in case of necessity. The PCB 901 is a standard size Eurocard (160x100mm).

In operation, each of the 3-terminal regulators (IC1, IC2, IC3, IC5) contains a bandgap voltage reference (between the output and the adjustment terminal), which generates a nearly constant voltage VREF of 1.25V (typical) over a large temperature range. The output voltage of 5V is set by P1; the output voltage of 24V is set by P2; the output voltage of + 15V is set by P4, and the output voltage of – 15 V is set by P3.

Another way to look at the regulators considers them as amplifiers of the voltage between the terminal 1 and ground as input, and terminal 2 as output. Since the voltage at terminal 1 is a fraction of the output voltage, the ripple of the output voltage will be amplified also. To minimize this effect, the filter capacitors C4, C10, C15, and C20 are inserted. To avoid a discharge of these capacitors through the regulators, which would cause malfunction of the regulators after a short circuit on the output, the diodes D3 and D1 are inserted.

Fig. 6.1.3:

Standard application of a LM 317.



$$V_{out} = \frac{V_{ref}}{R_a} (R_a + R_b)$$

$V_{ref} = 1.25$ V

R_a usually 240 Ω

For the 5V and 24V supply these discharges can go through R1 and R6, respectively. The diodes D4 and D2 prevent discharging of external and internal filter capacitors into the regulator circuit. The capacitors C1, C6, C12, and C17 serve for additional noise filtering. G1 to G4 are rectifier bridges, C2, C7, C13, and C18 are energy storage capacitors, and C5 and C11 are filter capacitors. A minimum load current for every supply is provided by R3, R8, R13, and R17. To guarantee proper function of the regulators this minimum load current must be large compared to the adjustment current (less than 100 uA) from terminal 1.

All power voltage regulators are thermal-overload protected and short circuit proof. For further details see attached data sheets.

5 V supply: The fuse F (2.5 A fast) is inserted to protect the regulator if an overvoltage protection circuit (crowbar circuit) should be built in. The fuse can be bypassed if necessary.

24 V supply: To avoid dangerous voltages (40V) at the regulator input, a pre-regulator is used. It consists of the Darlington transistor T1, the Zener diode VR1, and the resistors R4 and R5. Capacitor C8 prevents oscillations in that circuit.

± 15 V supply: These supplies are mainly used in analog circuits requiring great stability. The stability is achieved by the insertion of additional LM723 voltage regulators (IC4 and IC6). Each regulator consists of a very stable reference voltage source, an error amplifier, a current limiter, and an output stage. The output of the voltage reference amplifier (normally 7.15V, temperature coefficient 0.003%/C°) is connected to the non-inverting input of the error amplifier. A fraction of the output voltage, set by P3, R11, R12 (-15V) and P4, R16, R18 (+15V) respectively, is connected to the inverting input and compared with the reference voltage; the rest is done by the LM723 components. The current limiter prevents the LM723 from overloading. For further details see attached data sheets.

BIN ASSEMBLY

The UNO bin is normally delivered in assembled form. In order to facilitate disassembling and reassembling if necessary (or, if the bin should be delivered as a non-assembled kit) use the drawing in Fig. 6.1.4. Assembling the low voltage power supply 901 requires the rear panel to be taken off. Special nuts are used for this panel.

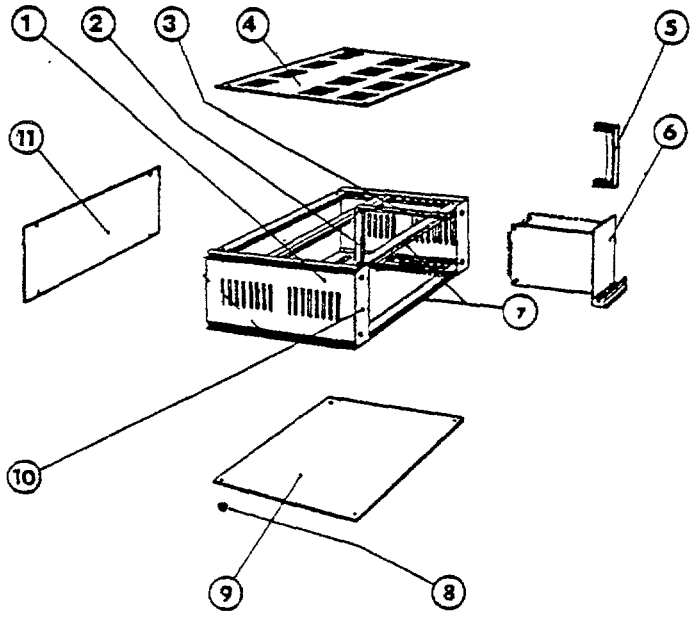


Fig. 6.1.4: Exploded view of the bin components.

1 side panel
2 connector
3 card guide
4 top cover
5 handle
6 front plate
7 supporting rales
8 rubber foot
9 bottom cover
10 handle supporting plate
11 rear plate

This laboratory power supply is based on an earlier IAEA Eurocard bin. Descriptions of the earlier unit are still useful, but several major changes have been made. The transformer is now mounted on the side panel, the power supply circuit board is internally mounted, and AC input and control is transferred to the front panel. Also the power supply output voltages are conveniently available on the front panel. This bins is designed to hold and to supply power to six single width plug-in modules.

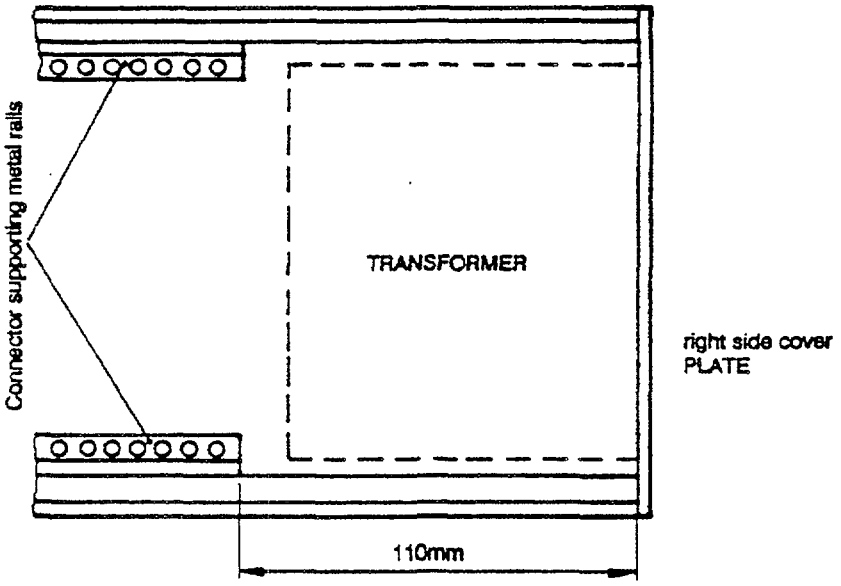
This power supply kit is very well designed, but it is not intended to be assembled by a novice. Explicit step-by-step instructions are not given. The builder is expected to use all his knowledge to produce a well constructed, easy-to-service unit. The circuit diagram is the basic guide to construction, but even it must be used with intelligence. For instance, the ground lead inside the supply from the line filter is not shown. Of course it must be connected to the chassis and separately to the front panel for it to provide its essential safety functions. Color code your wiring (suggestions will be made). Of course it makes no difference to the current whether it flows in a red or a blue wire, but it makes a big difference to the technician who is troubleshooting an inoperative supply. If all the wires were red, it would be impossible to trace them. To know that all, for example, yellow/green wires are connected to the chassis, is a great time saver. Use the sleeves provided when you connect wires. They make the final product look professional and provide useful short circuit protection.

Preparations

Remove the front, back, top, and side panel to which the transformer is to be mounted. Refer to Figs. 6.1.1 and 6.1.4. Part of the connector supporting rails have to be cut away to make room for the transformer. Cut as shown in Fig. 6.1.5.

Fig. 6.1.5:

Cuts to be made on connector rails to accomodate the transformer.



Mount the transformer to the side plate. Drill holes if necessary. Be sure the terminals are accessible with the top removed. Use four M3 x 10 screws, washers, lock washers, and M3 nuts to mount it. Put two solder lugs on the front upper screw. Re-attach the side panel with the transformer to the bin.

Next mount the card guides and the connectors.

Card Guides

Start with mounting the available plastic card guides by pressing them into appropriate slots in the supporting rails. The position of the card guides determines also the position of the bin connectors.

Mount the first card guide about 8 mm from the left side of the handle supporting plate (looking from the front; see Fig. 6.1.6). Insert the next guide at a distance of about 27 mm (6 teeth). The next card guide is a further 27 mm away, and so on. When you have installed all the guides, mount the connectors at their ends. This is done with M 2.5x10 screws and M 2.5 nuts. Finally, mount the top and bottom card guide for the power supply PCB. These guides should be in holes 55 and 56, counting from the left. No connector is needed for this card.

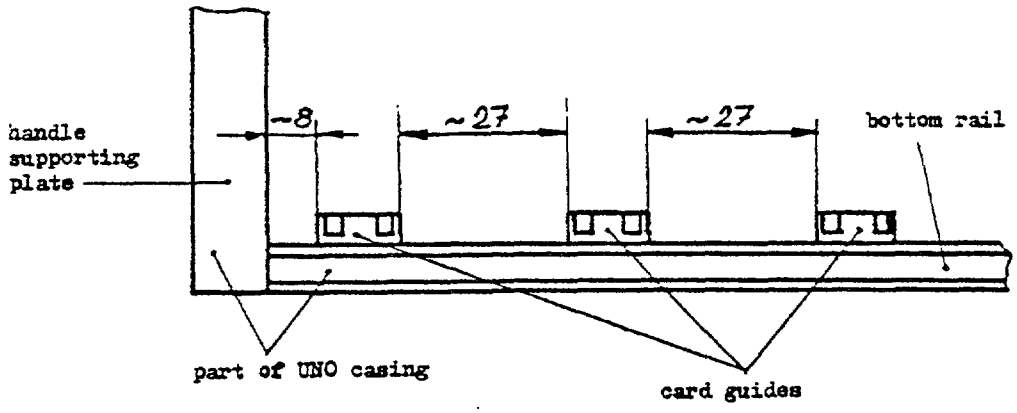


Fig. 6.1.6: Location of the card guides.

Bus Wiring

First straighten nine pieces of 1 mm^2 tinned wire, each about 300 mm long. For this purpose, fix one end with a pair of flat-nosed pliers. Pull strongly until the wire is streched by 3-5% of its original length.

Cut the wires to a lenght of 250 mm. Put them on the wire wrap connectors, starting from the right side (connector 1) of the bus looking from the rear. Fig. 6.1.7 shows the way the wires are to be connected. Note that the pin numbers are printed on the connectors.

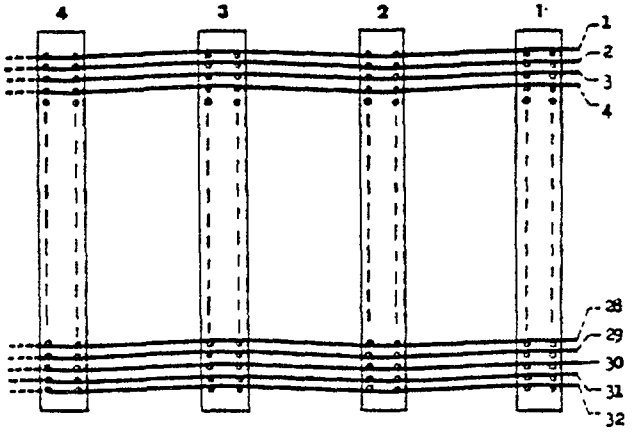


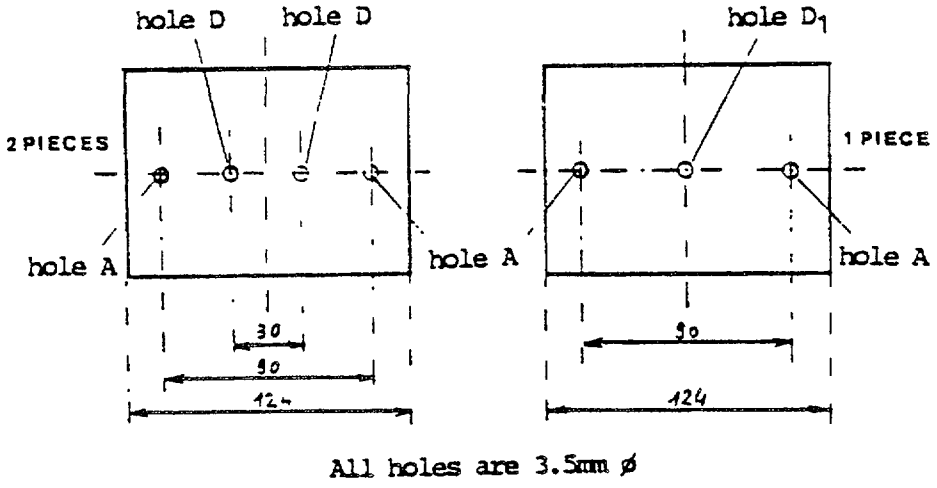
Fig. 6.1.7: Bin power bus wiring.

Rear Panel

Three heat sinks, two carrying two regulators and one a single regulator, are to be mounted on the rear panel. Figure 6.1.9 shows the drilling plan for the heat sinks.

Fig. 6.1.9:

Drilling plan for the heat sinks.



These heat sinks are usually predrilled. If they are not, take care when drilling the holes A that they match with the holes in the rear panel. For the location and position of the regulators on the heat sinks see Fig 6.1.10.

Fig. 6.1.10:

Location and position of regulators on heat sink.

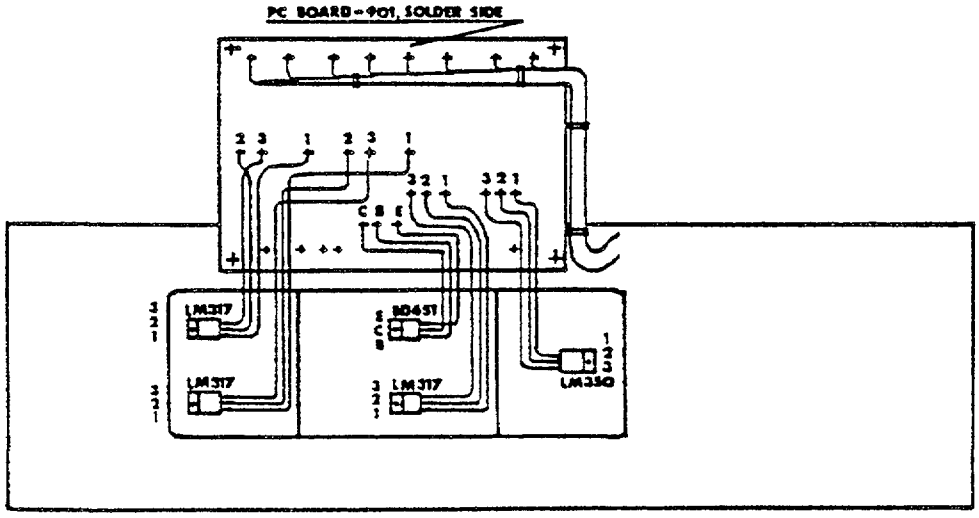


Figure 6.1.11 gives instructions on the method to be used to mount the regulators onto the heat sinks.

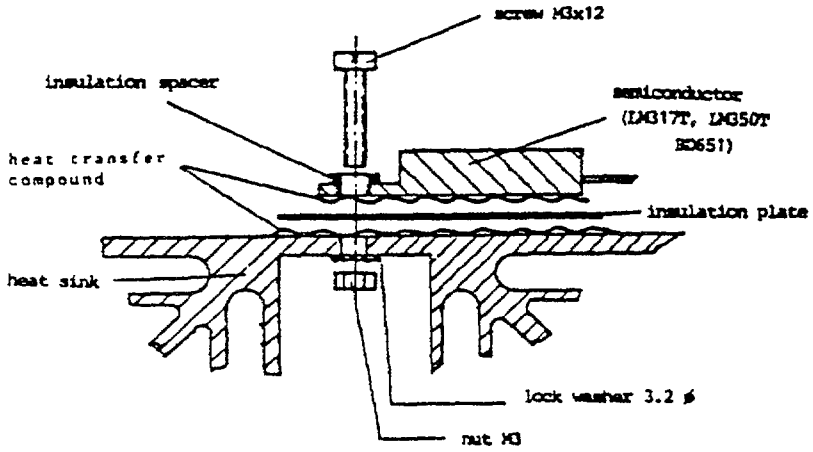


Fig. 6.1.11:

Detail of the mounting of a regulator on a heat sink.

Now mount the heat sinks onto the rear panel. Figure 6.1.12 provides some detail of this operation.

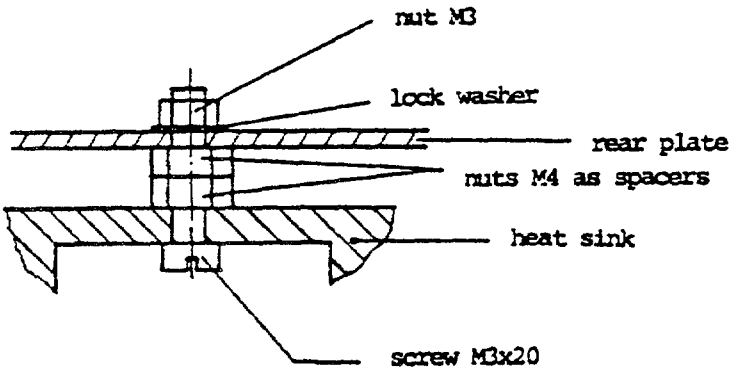


Fig. 6.1.12:

Mounting detail of heat sinks to rear panel.

Front Panel

The front panel holds the mains switch, the power connector and filter, and the banana jacks for external power connections. Figure 6.1.13 gives the details.

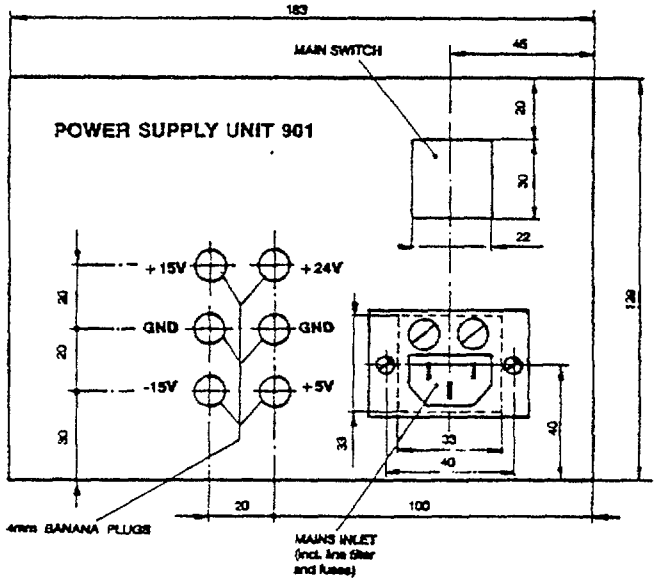


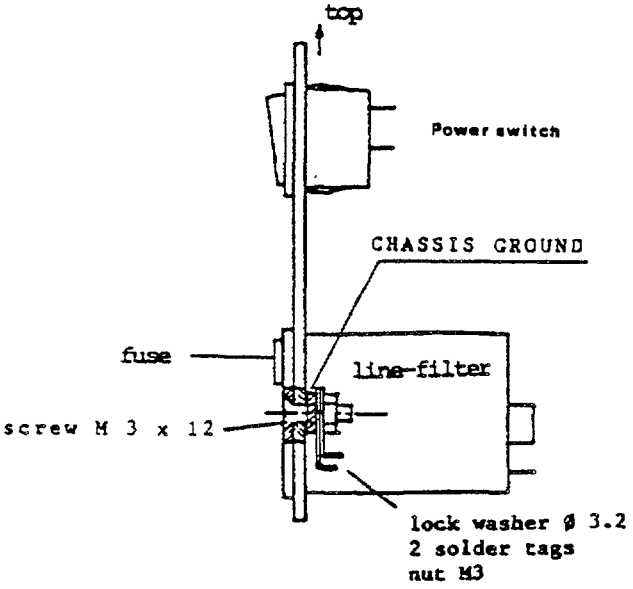
Fig. 6.1.13:

Front panel details.

Check the off position of the switch with an ohm meter. Press the switch into the prepared hole with the correct orientation. Mount the mains filter with two M3 x 12 screws with the fuses on the upper side. See Fig. 6.1.14.

Fig. 6.1.14:

Front panel assembly.

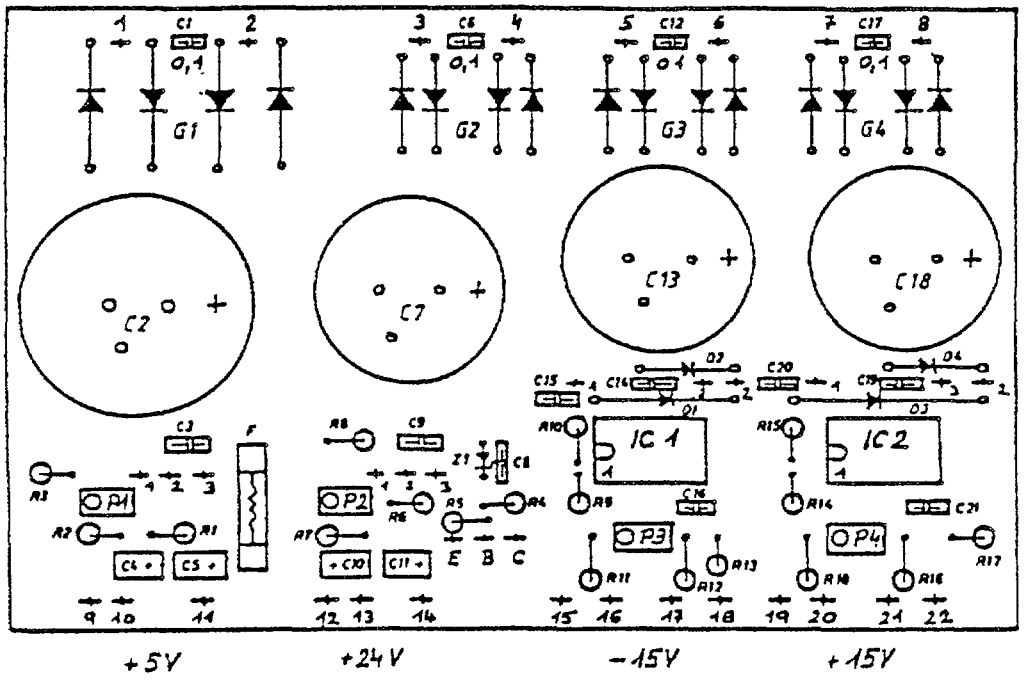


Place a lock washer and two solder lugs on the screw away from the near edge to provide a high quality (low ohmic) connection to the chassis ground (instrument case). Mount the banana plugs.

The parts layout diagram for the printed circuit board is shown in Fig. 6.1.15.

Fig. 6.1.15:

Component layout PCB 901.



Mount the solder lugs first. They go parallel to the long edge and should have their leads bent on the component side. See Fig. 6.1.16. There are 22 solder lugs for the numbered connections, 15 lugs for the regulators, and 4 lugs for the front panel banana jacks. These

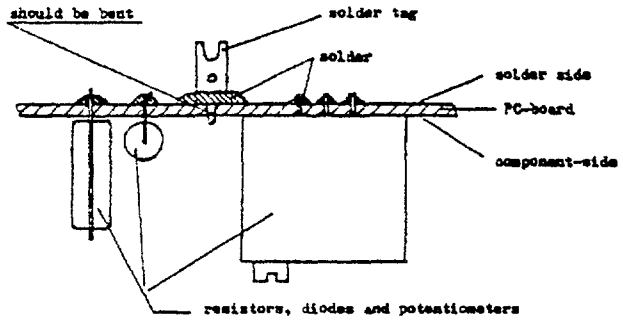


Fig. 6.1.16: Solder lug intructions.

last four lugs do not appear in the figure but holes are provided for them on the circuit board.

Next mount and solder the components in this order: diodes, resistors, potentiometers, and the big capacitors. (Note: the capacitors are not all the same.) Insert a few components at the same time, cover them with a sheet of thick foam (or other soft material) to avoid motion of the components when turning the board. Solder the components and clip the excess leads.

WIRING

Wiring will be done in stages. Use sleeves to cover all connections. A length of 25 mm will be enough in most cases. Some tests will be suggested occasionally to serve as a check on the wiring process. Color code your wiring and use cable ties to keep the wiring neat and easy to follow. Use lengths that are easy to cable and permit the parts to be disassembled without unsoldering. Place the rear panel behind the bin and the front panel and PCB in front to allow for easy length estimation. In general it is better to have the wire too long rather than too short.

Chassis Ground

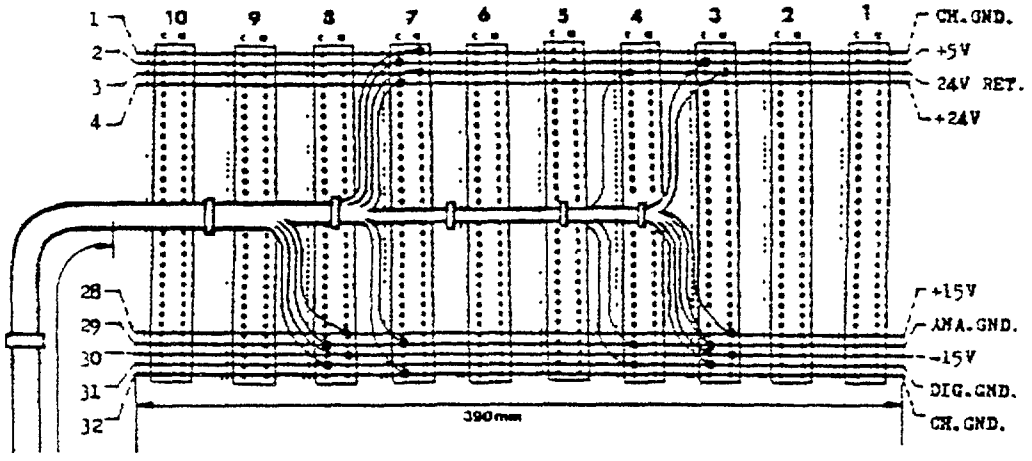
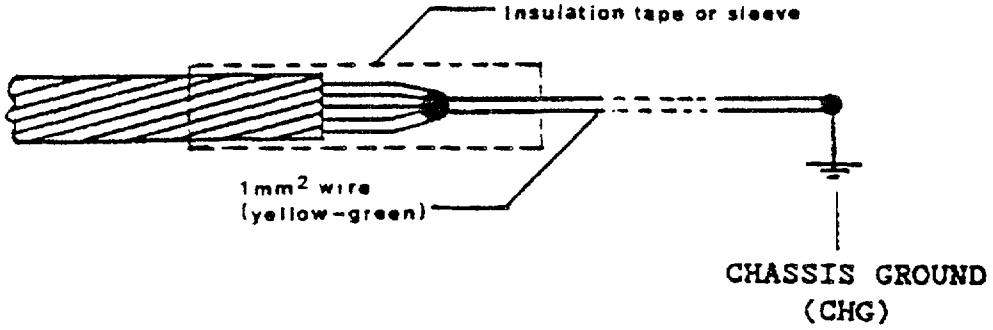


Fig. 6.1.17: Suggestions for connections to the bin bus.

Use yellow-green wire (about 60 cm long). Start with the bin bus. Figure 6.1.17 will suggest ways to connect these and the PCB wires to the bin bus. This figure cannot be used exactly, because it is drawn for a bin of 10 rather than 6 slots. But it does show the connecting wires distributed among the connectors to prevent crowded soldering conditions which might result in unintended shorts. Connect the five bus lines as indicated on the circuit diagram (Fig. 6.1.2) to one of the solder lugs on a transformer screw. Fig. 6.1.18 suggests a way to reduce these five wires to one.

Fig. 6.1.18:

Chassis ground connection.



Use cable ties to keep these wires together.

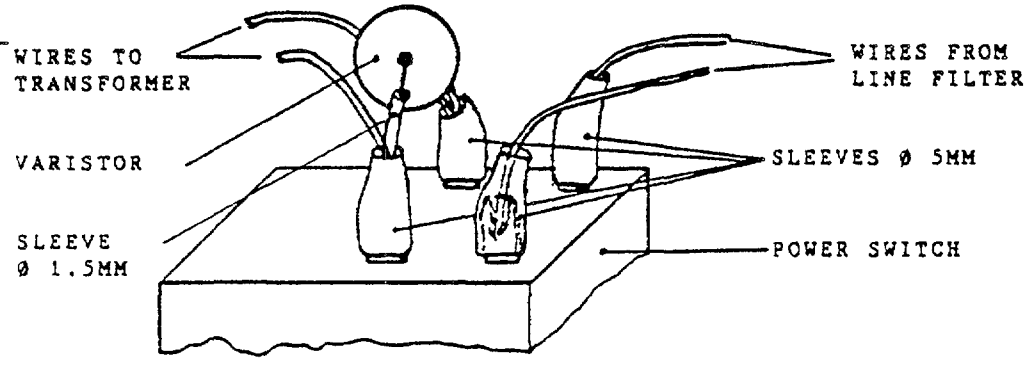
Connect the other solder lug at the transformer to the ground terminal of the filter. Connect the ground terminal of the filter to one of the solder lugs on the side of the filter. Connect the other solder lug on the filter to the near black banana jack. Connect that banana jack to the other black banana jack.

Front Panel

Now wire the mains switch and the filter. Refer to Fig. 6.1.19. Connect two red 1 mm^2 wires from the line terminals of the filter to the input of the power switch. Solder a varistor and two violet 1 mm^2 wires about 25 cm long to the other two terminals of the switch. Do

Fig. 6.1.19:

Wiring of power switch.



not forget the shrink tubing sleeves. Heat the sleeves to shrink them.

Now, make the following check. Insert the fuses (for fuse ratings, see circuit diagram), and connect the power cable to the input plug. Make a short circuit across the pins of the power plug and measure the resistance between the leads to the transformer with an ohmmeter. With "power on" you should get nearly zero ohms; with "power off" the resistance is 10M. If your results differ, isolate the trouble.

Attach a 1 mm^2 30 cm long wire to each of the remaining banana jacks. Red, blue, yellow, and green wires are suggested. Use cable ties to keep these wires together.

Transformer

First wire the primary of the transformer. Determine the average mains voltage of your laboratory during the working day and use the diagrams of Fig. 6.1.2 to connect the violet wires from the switch to the appropriate terminals. Use short jumpers too, if necessary.

Your transformer is now wired for one of six possible input voltages. Make a small label telling which you selected and tape it to the front panel near the mains input socket.

There is another difficulty. The varistor you placed across the switch is designed to clip noise spikes which often appear on the power line. It clips spikes larger than 275 volts and is, therefore, not very effective on power lines in the 120 volt range. If one were to replace the varistor used here with one designed for 120 VAC, this power supply could no longer be used on 220 VAC even with the transformer primary rewired. However, if a varistor with a 180 V max rating were placed across each of the two primary windings, the power supply would be well protected for any line voltage.

When this has been done you can check the secondary voltages by connecting the transformer to the mains via the line filter and power switch. Check that the secondary voltages are those indicated on the transformer, keeping in mind that they will be a bit higher without load. If everything is correct, you can proceed to the next step. The voltages measured with an AC voltmeter are the true ones, even if contrary to the lettering on the transformer. Trust your measurements, find the reason if the results of your check are unsatisfactory.

> WARNING: If your mains supply is not provided with a ground connector, you have to connect the ground wire of the mains cable to a proper electrical ground. This is necessary for reasons of safety and also to guarantee the correct operation of the power supply.

PCB

It is now easy to make the connections between the transformer and the PC board. Start wiring at the transformer terminals. Use 1 mm^2 wires of different colors for each winding, e.g. two violet wires from the terminals of the 11 V output. Make the wires long enough to reach the PC board when it is in front of the bin.

Use the circuit diagram to see how the secondary windings are connected to the terminals at the bottom of the PC board. Finally use cable ties to keep these wires together.

Next, proceed with the connections between the PC board and the regulators mounted on the heat sink. Make these connections step by step and check them with the circuit diagram. Cover all the soldered connections to the regulators with sleeves. All wire connections to the PC board must be made on the solder side. Use 1 mm^2 wires of different colors, red wires for regulator input, violet for output, and brown for the adjustable terminal. Make the wires long enough to go from the PCB in front of the bin, through the bin to the heat sinks on the back panel lying behing the bin, Use cable ties to keep these wires together.

Connect the wires from the banana jacks on the front panel.

Now you can start with the electrical pre-check. First, connect the following terminals with small pieces of wire: 9 and 10, 12 and 13, 15 and 16, 17 and 18, 19 and 20, 21 and 22.

Connect the power supply to the mains and measure the voltages between the following terminals with a DC voltmeter.

Terminal	Meter reading
9 - 11	5 V
12 - 14	24 V
15 - 18	15 V
19 - 22	15 V

Small corrections can be made by adjusting the potentiometers P1 to P4. If this is not sufficient, then check the PC poard for errors and do some trouble shooting.

Now for the interconnections between the PCB and the bin bus. Keep in mind that you want a low voltage drop across these connection lines. Therefore, solder carefully, and use heavy gauge wire for the DC power and chassis ground lines. Use 0.38 mm^2 wires for the sense lines. If possible, use wires of different colors. Figure 6.1.17 will suggest line routings. Start by soldering seven lines, including the sense lines, to the pins of connector 1. Use cable ties to form the cable harness. Cover the solder points at the wire wrap pins with sleeves which have a length of about 25 mm. Note that two +5 V wires are used to minimize the voltage drop to the bin bus if high current is drawn.

FINAL STEPS

Calibrate your power supply. Connect a DVM (digital voltmeter, if possible 4 1/2 digits) to the bus lines (select the related ground line) and adjust the output voltage of the different supplies to their specified values. Check the ripple. (Use a 1:1 oscilloscope probe.)

Then solder heavy gauge wires to the floating end of the bin bus lines and load the different supplies with the maximum current (use heavy power resistors). Verify the specifications given at the beginning of this project.

Now for the final assembly. Remove the temporaty wires to the test load and insert the PCB into its bin slot (the one without any connector). Next attach the front and rear panels. Put the top back on, and your power bin is complete.

There are still features of the power supply which have not been discussed and which are hard to learn about from the circuit diagram only.

Note that the connections between the bin power bus, the sense lines, and the banana jacks are such that, if the power bus is heavily loaded, the banana jack voltages will be slightly higher than usual. The additional voltage will be about 20 mV/A and is negligable in normal applications. When using the banana jacks, be sure you do not exceed the current ratings of the power supplies. Also note that the return current from the banana jacks use the chassis ground lines. This arrangement simplifies the wiring a bit at the expense of regulation and good wiring practice.

Special project 6.2

HIGH VOLTAGE POWER SUPPLY: 0 - 2000 V, NEGATIVE

OBJECTIVE

A high voltage power supply to be used in biasing the x-ray detecors with optical feedback preamplifiers will be designed and constructed. The complete instructions are given.

REVIEW

When biasing of silicon semiconductor detectors, a power supply for up to -2000 V and at few μA is required. This small current consumption allows the construction of a power supply based on transforming a sinusoidal voltage instead of a rectangular one. The advantage of such power supply is the reduced interference by high frequencies harmonics which are present in the rectangular shaped signals.

The basic block diagram of the high voltage power supply is given in Fig. 6.2.1. The sinusoidal voltage produced by the sine wave oscillator provides power for the transformer through the analog multiplier whose gain is determined by U_o. The α -part of the high voltage U_o is compared with the reference voltage U_{ref}. The difference is multiplied by G, in the analog amplifier.

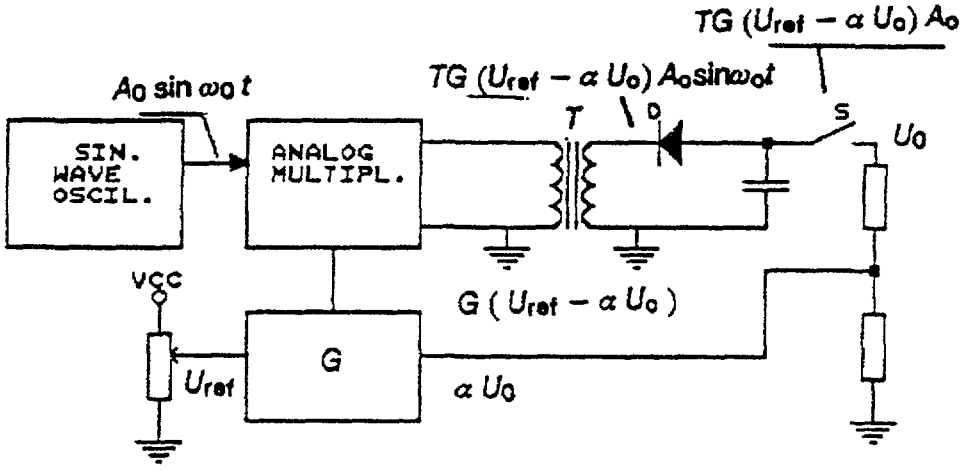


Fig. 6.2.1: Initial version of the high voltage power supply.

We can find the relation between U_o and U_{ref} if we consider the circuit at point P open, and follow the signals around the open loop.

Starting from voltage U_o, the rectified voltage is A_o T.G. α $(U_{ref}-U_o)$ (T is the transformation ration.). When we close the circuit again, we must have:

$$M\, A_o\, G\, (U_{ref} - \alpha\, U_c) = U_o$$

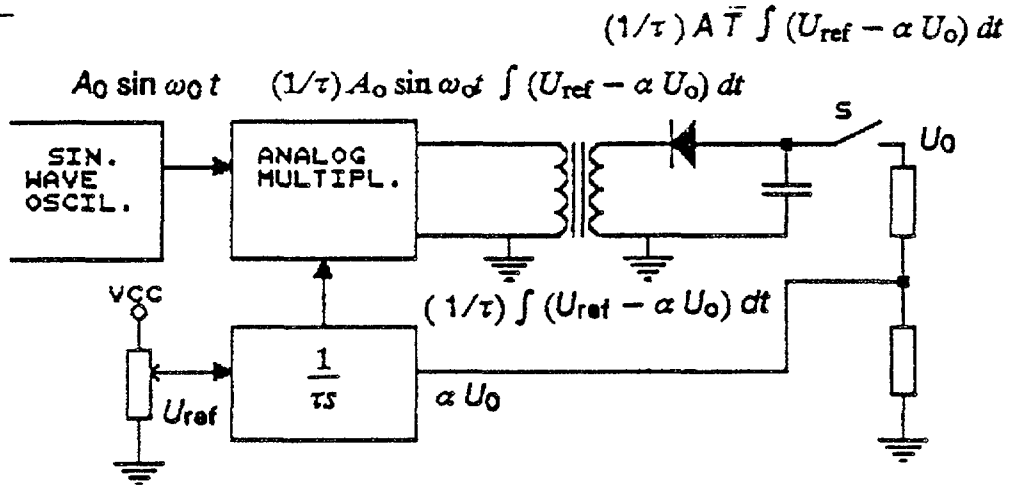
At high gain G, the above relation is simplified to:

$$U_{ref} = \alpha\, U_c \quad \text{or} \quad U_c = \frac{U_{ref}}{\alpha}$$

However, the circuit shown in Fig.6.5.1 would oscillate. Instabilities are caused by the high gain G, and the unsufficient smoothing of U_o after the rectification. This problem can be eliminated by introducing integration in the feedback loop instead of straight amplification (Fig. 6.2.2).

Fig. 6.2.2:

Integral regulation improves stability



In this case the regulation equation is:

$$A_o \frac{1}{\tau\, s} (U_{ref} - U_o) = U_o$$

After rearranging, we can write:

$$U_o = \frac{1}{1 + \tau\, s} U_{ref} \quad \text{or} \quad U_o = \frac{1}{1 + \tau'\, s}\, U_{ref}$$

This equation predicts that the asymptotic solution, for constant U_{ref}, is $U_o = U_{ref}$. If U_{ref} is changed, U_o will follow U_{ref} with a time lag. If the system has been disturbed, the U_o will approach to U_{ref} exponentially with the time constant τ .

Several additional modifications can be introduced to improve the featires of the power supply.

- To avoid the insulation problem at the transformer secondary coil, a voltage multiplying circuit circuit will be used. For safe operation the transformer secondary voltage should not exceed 600 V.

- To avoid a high transformer ratio, the primary windings of the transformer receive power from two amplifiers with output voltages of opposite phases:

  $A_o \sin \omega t$ and $-A_o \sin \omega t$.

- The sinusiodal voltage is produced from the clamped triangular voltage. The triangular voltage is generated by the relaxation oscillator. In this way the frequency can be adjusted by a simple potentiometer over a wide range. The proper frequency adjustment allows to optimize working conditions.

- When the high voltage is applied to a semiconductor detector, the recommendation is that this should happen slowly, at a rate not faster than 100 V/s. To avoid fast changes of the output voltage an additional circuit is introduced (see Fig. 6.2.3).

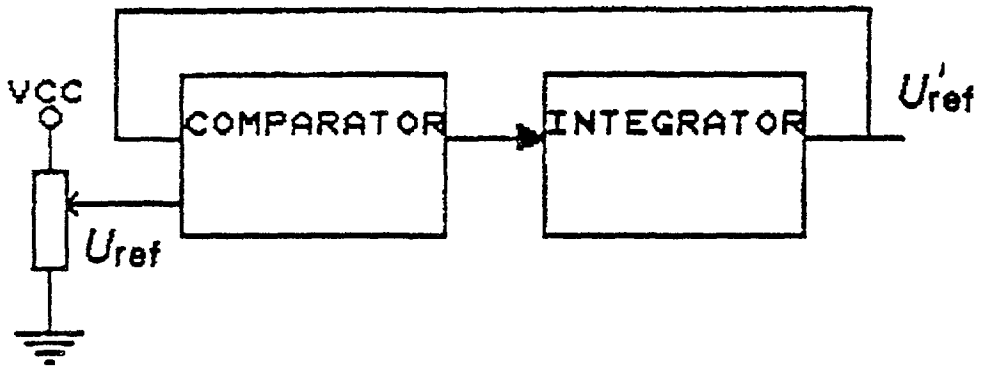


Fig. 6.2.3: Circuit for slow voltage increase

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Let us consider the case when the output U'_{ref} is zero, and U_{ref} is instantaneously changed to 5 V. Comparator will responde with a saturated output voltage which remains constant until U'_{ref} will reaches U_{ref}. During this time the integrator output voltage U_{ref}' will rise linearly because the voltage at the integrator input. The slope will depend on the time constant of the integrator.

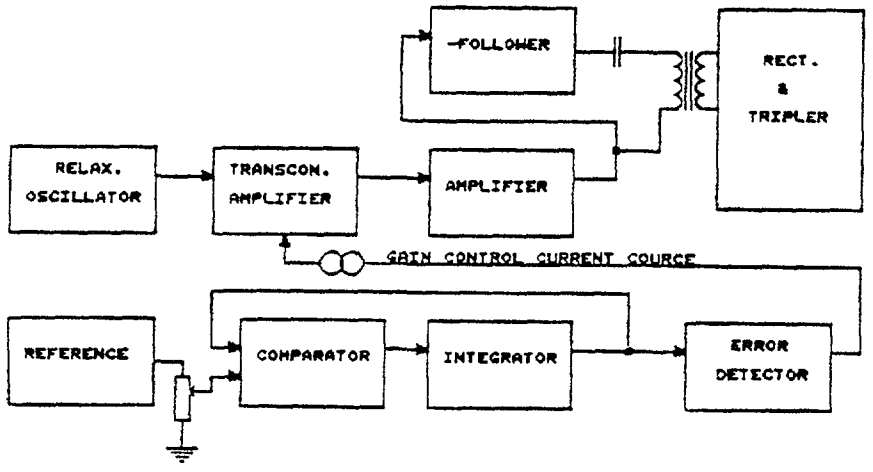


Fig. 6.2.4: Block diagram of the high voltage power supply.

Now we can understand the final version of the high voltage power supply presented in the block diagram in Fig. 6.2.4, and in the detailed wiring diagram shown in Fig. 6.2.5.

The relaxation oscillator provides the triangular voltage of 300 mV peak to peak to the inverting input of the IC4, pin 2. This voltage is applied to the transconductance operational amplifier IC5 CA3080. The amplification is controlled by changing the current

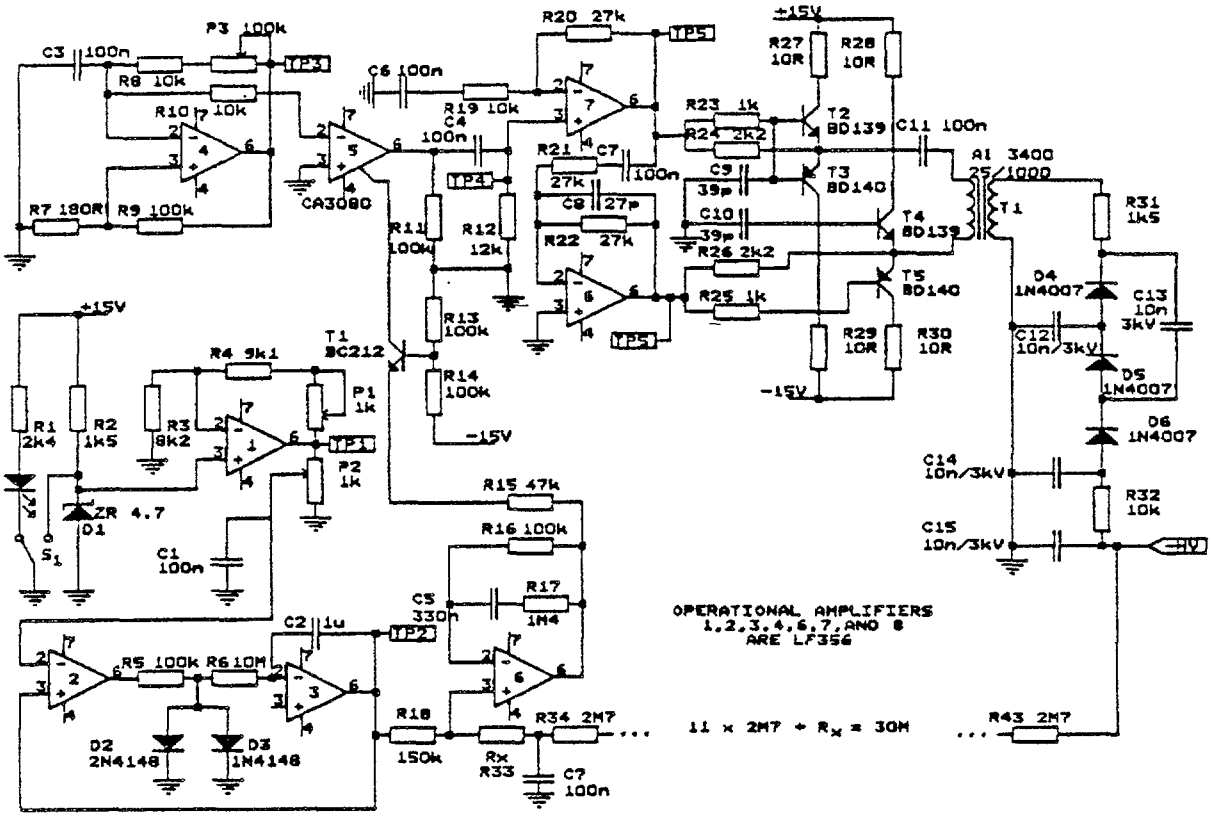


Fig. 6.2.5:

Wiring diagram.

into pin 5. The output current of the transconductance amplifier is converted into a voltage by using resistor R12. Any possible DC component is removed by C4. Because of the saturation of the CA3080 for large input signals the output signal is clamped. The resulting signal of sinusoidal shape, with amplitudes from 0 to 5 V, is amplified by a factor of about 2, by using IC7, and inverted into the IC8. Both amplifiers are buffered by two identical emitter follower output stages. These are connected to the primary coil of the HV transformer.

The voltage on the secondary side of the transformer is rectified and multiplied by a factor 3. A fraction of the DC voltage is compared with the reference signal U_r in IC6. One part of the differencem is amplified, and one part is integrated within the same IC (proportional and integral regulation). The voltage error signal is converted into the current error signal by using transistor T1, injecting the current into CA3080, pin 5.

The 10 V reference signal is produced by IC1. The primary reference is a 4.7 V Zener diode connected to 15 V via R2. The reference voltage is set to 0 in the OFF state of the switch SW-1.

The required high voltage is set by a ten turns potentiometer P2. By using the comparator and integrator within the negative feedback loop the response of the control voltage U ' to the control voltage U_c is slowed down to the 1 V/s. That is equivalent to 100 V/s for the high voltage output.

Assembling and testing

EXPERIMENT

Assemble the printed circuit board according to the wiring diagram, leaving IC6 out..

Put a 100K resistor with legs into holes 2 and 6 of the IC6 (see Fig. 6.2.6).

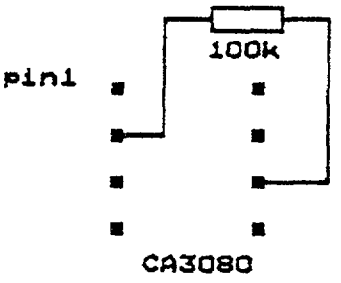


Fig. 6.2.6: Disabling the feedback loop.

Record the signals at TP3, TP4 and TP5. Use P3 to set the the frequency by P3 to get the maximum voltage across C12. Remove the auxiliary resistor, insert IC6 and finish the voltage tripler.

To calibrate the HV output, set P5 to 5.0 V and adjust trimpot P1 until the output is 500 V as read by an external meter.

In the case of trouble you can check the operation of the separate stages by using testpoint TP1 to TP5.

- TP1: DC voltage, very close to 10 V. Depends on the Zener reference voltage. P1 varies the voltage at TP1 for about 10%.
- TP2: DC voltage equal to TP1 value x P2 setting (one half of TP1 voltage if P2 is at 5.00; equal to TP1 value if P2 is 10.00).
- TP3: rectangular signal, swinging between 14 and -14 V. Frequency can be changed from 1 to 10 kHz.
- TP4: clamped triangular signal similar to the sinusoidal voltage. Amplitude proportional to the P2 setting.
- TP5: about 4 times amplified TP4 voltage.

Notes:

Special project 6.3

GEIGER-MUELLER RATEMETER

OBJECTIVE

To assemble and test a simple ratemeter to be used with a Geiger Muller counter.

REVIEW

The mean count rate of pulses withA randomTIME distribution such as the pulses coming from nuclear radiation detectors, can be measured with integrating type ratemeters, displaying the count rate on an analog meter.

The circuit (see Fig.6.3.1) is composed of a simple high voltage power supply for biasing the GM counter and an circuit to develop a voltage proportional to the count rate.

The high voltage power supply is similar to the one described in the Power Supply series of this manual.

The ratemeter works as follows: each time the GM delivers a pulse, the one-shot circuit is triggered and produces a pulse having a standardized width (approx. 780 us) and 15V amplitude. A current pulse is injected into the operational amplifier used as an integrator circuit. In equilibrium state, that is to say at constant count rate, a constant voltage is developed at the output of the operational amplifier. (The feedback resistor R_F as R_1, R_2 or R_3.)

$$V_0 = i \cdot R_F \qquad \text{(Eq. 6.3.1)}$$

Here i is the current circulating through RF, equal to the average injected current i_{av}.

$$i_{av} = \frac{V}{R_4 + R_{17}} \cdot t_w \cdot r \qquad \text{(Eq. 6.3.2)}$$

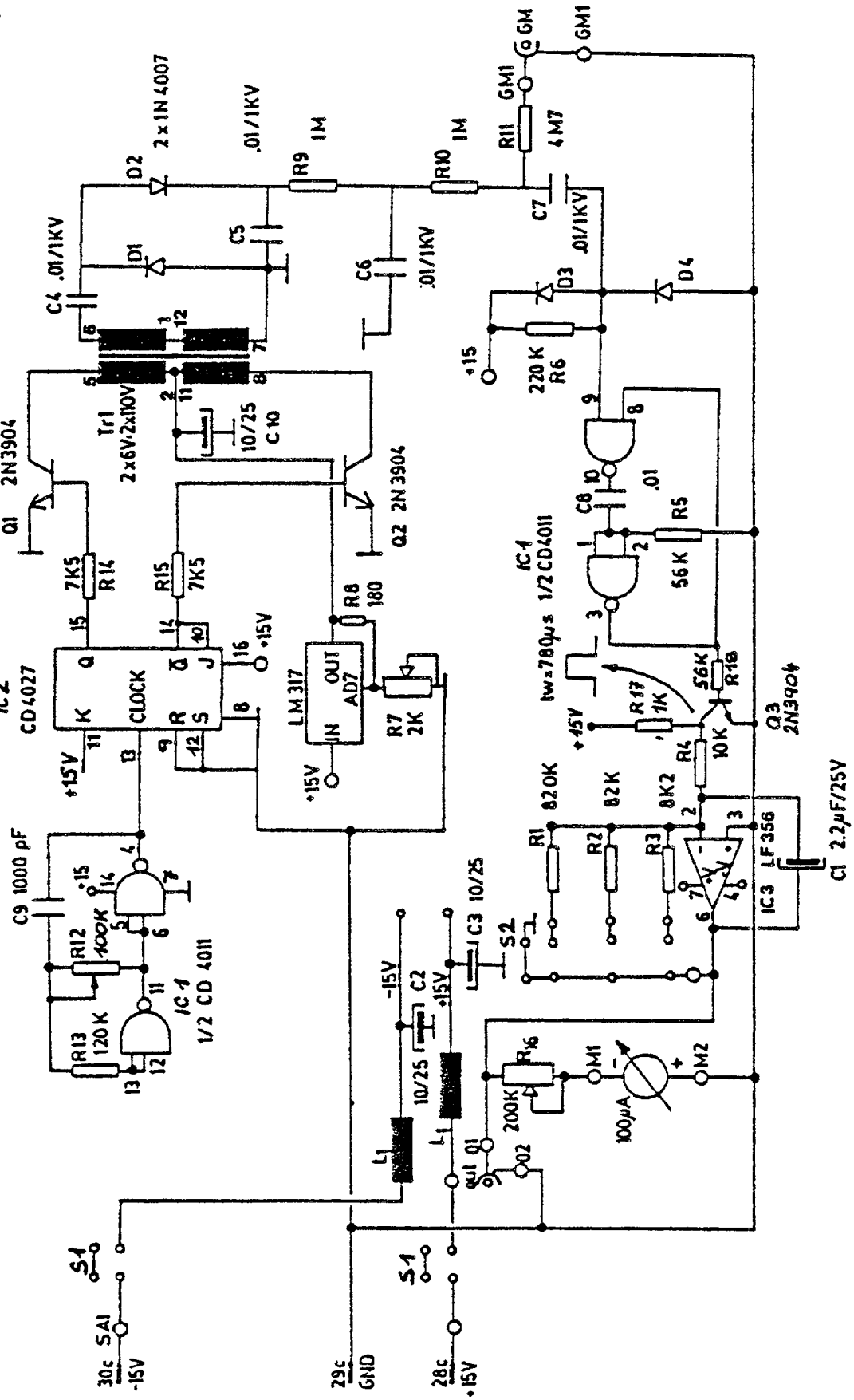
where: V is the height of the pulse (15V)
tw the width of the pulse (780 us)
r the count rate.

Combnining Eq.6.3.1 and Eq.6.3.2 we get

$$V_0 = V \cdot t_{ww} \cdot \frac{R_F}{R_4 + R_{17}} \cdot r \qquad \text{(Eq. 6.3.3)}$$

Fig. 6.3.1:

Circuit diagram of Geiger Mueller ratemeter



Observe that C_1 does not appear in the expression of V_0 but its value has to be such that the time constant $R_F C_1$ is much greater than the inverse of the count rate 1/r.

In our case three different values of R_F can be selected with a switch in order to get three different scales:

$V_0 =$ 10V at 1000 pps then $R_F = 8K2$
$V_0 =$ 10V at 100 pps $R_F = 82K$
and $V_0 =$ 10V at 10 pps $R_F = 820K$

These values are obtained considering that according to equation Eq. 6.3.3

$$R_F = \frac{V_0 \cdot R_l}{V \cdot t_w} \cdot \frac{1}{r}$$

$$R_F = \frac{10 \cdot 10^4}{15 \cdot 780 \cdot 10^{-6}} \cdot \frac{1}{r}$$

$$R_F = 8.5 \cdot 10^8 \cdot \frac{1}{r}$$

An analog meter indicates the count rate by measuring the operational amplifier output voltage.

Assembling instructions

The circuit diagram for the GM ratemeter is given in Fig. 6.3.1, the suggested components layout is seen in Fig. 6.3.2.

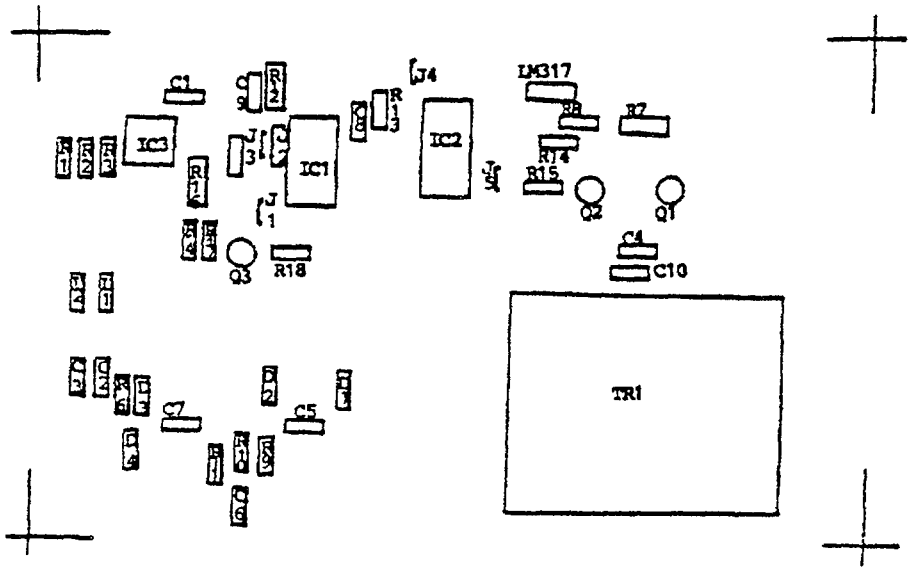


Fig. 6.3.2: Component lay-out for the Geiger Mueller Ratemeter

EXPERIMENT

A. Ratemeter

- Mount the monostable, the operational amplifier and related components on the circuit board.
- Apply negative pulses through C7 from an external generator.
- Check that the pulses produced at the monostable output have a width of 780 ms and an amplitude is 15V.
- Check that the output voltage changes with frequency.
- Adjust R16 to get the proper full scale indication for each range.

B. High Voltage Supply

- Mount on the printed circuit board the oscillator, flip-flop, transistors Q1 and Q2, transformer and voltage regulator.
- Check the frequency of oscillation, and see that transistors Q1 and Q2 reach saturation.
- Check that the voltage on the center tap of the transformer can be adjusted by means of R7.
- Mount the rectifiers and the high voltage components.
- Measure the range through which the high voltage can be varied by adjusting R7.

Geiger Müller Counter

- Connect the GM tube to the printed circuit board (don't forget to ground the cathode of the tube).
- Observe the pulse shape at the input of the monostable circuit.
- Observe the output voltage indication for different intensities of radiation.

MODIFICATIONS

This circuit does not operate perfectly. Of course no circuit does. What are its major defects? Is the output stable? Do you get the same readings for the same source on different ranges? Are all the ranges linear? Does the meter read zero with no source present?

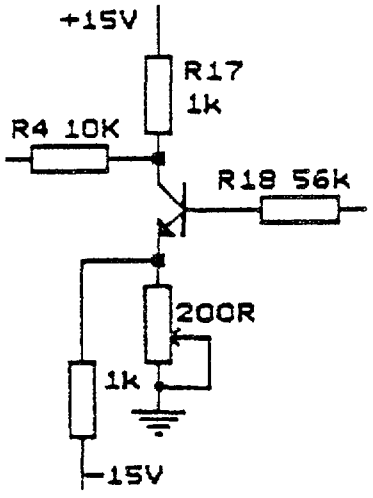


Fig. 6.3.3: Zero adjust circuit for meter.

Consider the last question. Why is the reading not zero? What does Q3 have to do with this question? What is the function of Q3? Why does the collector voltage never become zero?

One suggestion for zeroing the neter is to replace the circuit of Q3 with that shown in Fig. 6.3.3.

Here the emitter is made to go to a negative voltage so that the minimum collector voltage can better approch zero by putting a 200 ohm trimmer from the emitter to gound and a 1K resistor from the emitter to - 15 V.

What other ways can be used to more nearly zero the meter? What about a diode in the collector output of Q3? An adjustible connection on the non-inverting input of the op amp? An input offset circuit for the IC?

Returning the meter to a positive voltage? Using a digital inverter for Q3? Write out these circuits and try as many of them as you can. List their advantages and disadvantages.

Another easy modification will permit the precise adjustment of the pulse width. Replace resistor R5 with a 100K trimmer.

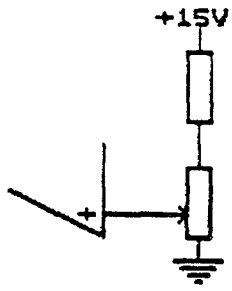


Fig. 6.3.4:

Alternative meter zeroing circuit.

Notes:

SPECIAL PROJECT 6.4

SINGLE CHANNEL ANALYZER

Single channel analyzer (SCA) is assembled using a prefabricated PCB and then tested. You are asked to complete documentation by measuring voltage levels and waveforms at the test points..

OBJECTIVE

A SCA is a device providing an output pulse of constant amplitude and duration if the input receives a pulse greater than V_1 and smaller than $V_1 + V_2$.

REVIEW

Thed single channel operation can be achieved by observing input pulses with two discriminators, one set at V_1 and $V_1 + V_2$. If V_1 is exceeded by the input pulse then the one shot providing the output pulse is activated. If $V_1 + V_2$ is exceeded, the activation of the one shot is inhibited. The voltage V_1 is usually called the level, and voltage V_2 is called the channel width.

A block diagram of a SCA is shown in Fig. 6.4.1. Various waveforms from the circuit are given in Fig. 6.4.2.

Instead of comparing the input signal V_i with V_1, the voltage V_1 is subtracted from the input signal in the differential amplifier. The resulting voltage is compared with zero in the ZERO LEVEL DISCRIMINATOR. This voltage is also compared with V_2, the UPPER LEVEL DISCRIMINATOR. The output of the discriminator is active if the incoming pulse is greater than V1 + V2.

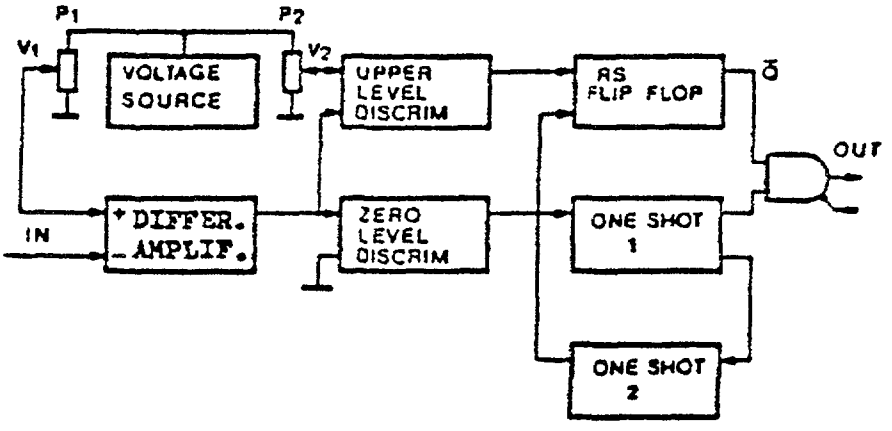


Fig. 6.4.1: SCA block diagram

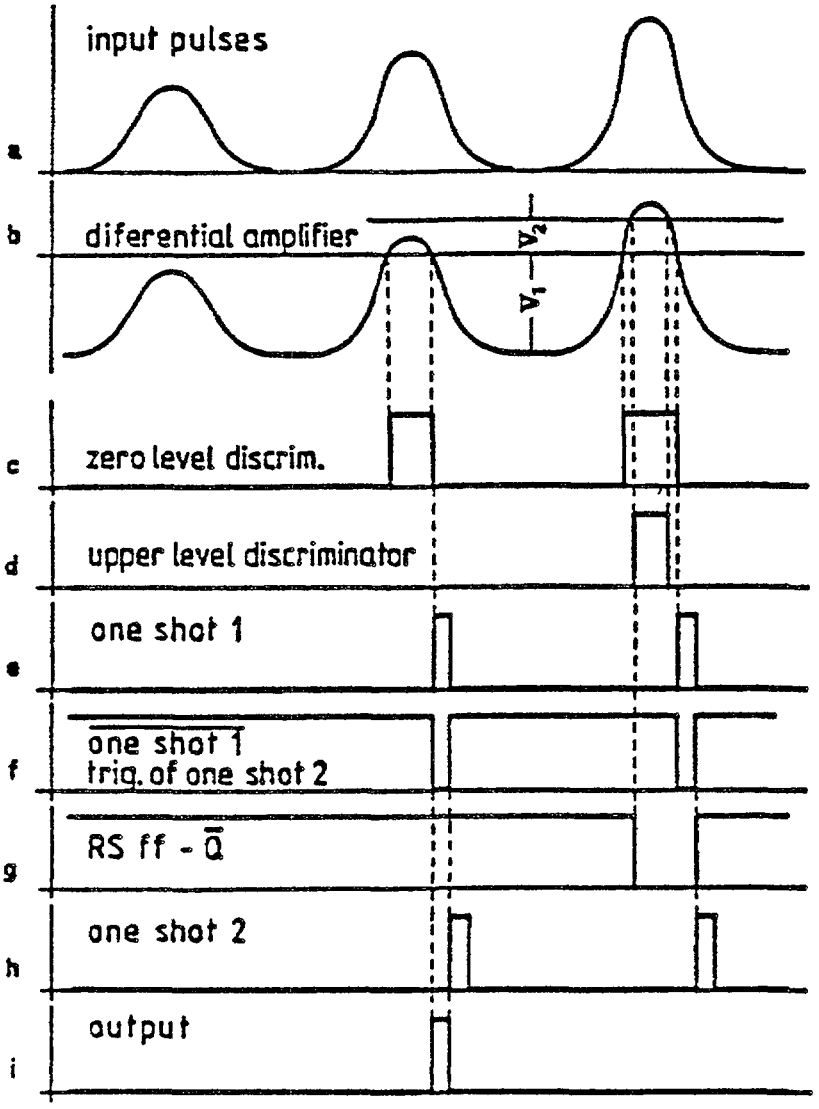
With respect to the height of the input pulses three different cases will be considered.

In the first case the input pulse (Fig.6.4.2a) is smaller than V_1. The resulting voltage does not exceed zero (Fig. 6.4.2b). Neither the ZERO LEVEL DISCRIMINATOR nor the UPPER LEVEL DISCRIMINATOR set at V_2 are activated.

In the second case the resulting voltage exceeds zero but does not exceed the V_2 of the upper level discriminator. The ZERO LEVEL DISCRIMINATOR is activated (Fig. 6.4.2c). The ONE SHOT 1 is triggered by the falling edge of the zero level discriminator(Fig. 6.4.2e). This positive going pulse is transmitted through the 2-input AND gate (Fig. 6.4.2i) because the Q output of the RS flip-flop is 1 (Fig.6.4.2g). Finally,the falling edge of ONE SHOT 1 output pulse (Fig. 6.4.2f) activates the ONE SHOT 2 (Fig. 6.4.2g). However, its positive going pulse intended for the RS flip-flop reset is meaningless.

Fig. 6.4.2:

Signal Forms



In the third case the input pulse is greater than $V_1 + V_2$. After being shifted down in the DIFFERENTIAL AMPLIFIER by V1, the pulse amplitude is still greater than V_2 level. Therefore both discriminators are activated (Fig. 6.4.2c and 6.4.2d). First, by the positive going pulse from the UPPER LEVEL DISCRIMINATOR (Fig. 6.4.2d) the RS flip-flop is set, resulting in Q = 0 state (Fig. 6.4.2g). Then, as in the previous case, the ONE SHOT 1 is triggered (Fig. 6.4.2e) by the 1 → 0 transition of the ZERO LEVEL DISCRIMINATOR (Fig. 6.4.2c). The pulse from the ONE SHOT 1 is stopped in AND gate due to Q = 1 state at one input of AND gate. By the end of the ONE SHOT 1 pulse the ONE SHOT 2 is triggered (Fig. 6.4.2h). The produced pulse resets the RS flip-flop (Q = 1; Fig. 6.4.2g).

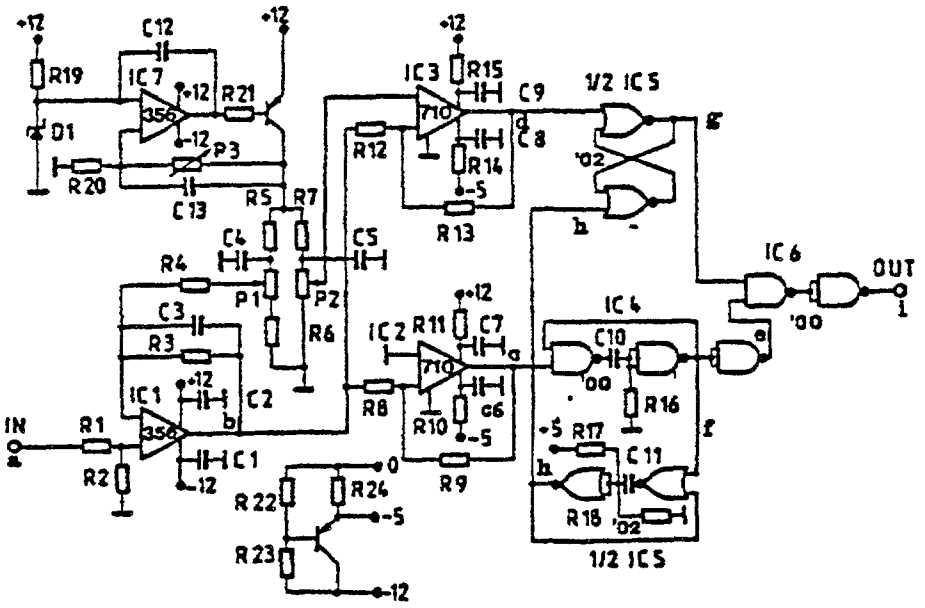


Fig. 6.4.3:

Scheme of SCA

The detailed SCA scheme is shown in Fig 6.4.3.

The SCA input stage (IC1) is a differential amplifier with different input sensitivities. To the inverting input with the amplification factor 1 the reference voltage V_1 from potentiometer P1 is connected. This voltage can vary from 50 mV to 5V. The smallest voltage, 50 mV, is determined by resistor R6, and the biggest voltage 5V is the voltage of the voltage source with IC7. By the voltage drop across R6 the threshold voltage of 100 mV for input pulses is introduced. Through two RC filters R5, C4 and R7, C5 voltages V_1 and V_2 are decoupled.

Pulses to be analysed are applied to the noninverting input of IC1. They are attenuated by a factor of 2 determined by the proper ratio of resistors R1, R2, R3 and R4; and shifted down for V_1. By adjusting the capacitor C3, made of two twisted wires, the optimal pulse response of the input stage is achieved. For this purpose rectangular input test pulses of a few μs have to be attached to the input.

Through the described attenuation the input pulses normally swinging between 10 and - 10 V are reduced to ± 5 V in height. This is the normal operating range for fast differential comparators IC2 and IC3 (SN 72710). In order to avoid interference, each 710 is supplied with its own RC filter at supply lines.

The negative edge triggered ONE SHOT 1 accepting signals from IC2 is formed from 2 NAND gates of 74L200. Capacitor C10 and resistor R16 are chosen to provide an output pulse of the duration of 1 μs. As the output pulse at pin 8 of IC4 is negative going, an inverter is added.

In the positive edge triggered ONE SHOT 2, two NOR gates from 74L201 are utilized and the DC voltage at input pins 11 and 12 of IC5 is reduced to 2.5V by the resistor dividing network R17 and R18. Reliable triggering by the negative going pulses of the amplitude 3.5V obtained by the differentiation of 1 0 transition of pulses from the previous stage, is assured in this way.

Suggested Components

C1	100n	R1	3K
C2	100 n	R2	1K
C3	twisted wires	R3	5K
C4	0 .22 u	R4	56K
C5	0 .22 u	R5	33 R
C6	100 n	R6	15 R
C7	100 n	R7	33 R
C8	100 n	R8	470 R
C9	100 n	R9	100 K
C10	4.7n	R10	100 R
C11	1 n	R11	100 R
C12	10 p	R12	470 R
C13	47p	R13	100 K
C14	0.22u	R14	100 R
C15	0.22 u	R15	100 R
		R16	360 R
		R17	5kl
P1 1k, ten turns		R18	5kl
P2 1k, ten turns		R19	1k5
		R20	56 K
P3 10k, trim pot		R21	100 K
		R22	6k8
		R23	6k8
Tr 1, Tr 2 BC 212		R24	15 K
DI ZR 4.7			
IC 7 LF 356			
IC 2, IC 3 SN 52710			
IC 4, IC 6 SN 74LS00			
IC 5 SN 74LS02			

In order to make the operation of the SCA independent of the supply voltage which may vary from bin to bin the internal reference voltage is used. The 4.7 V reference voltage provided by ZR 4.7 (D1) is increased to 5 V in the noninverting amplifier with IC7 by using the proper R 20/P3 resistance ratio. Transistor Tr1 is added to increase the current output capability of the voltage source.

Transistor Tr 2 connected as the emitter follower provides -5V for 710 drive.

EXPERIMENT

1. Assemble the single channel analyser board, according to the wiring diagram (Fig. 6.4.3). The component layout diagram (Fig. 6.4.4) will be useful.

2. Apply the pulses from a pulse generator, and observe the shape and the timing of the signals at the testing point a - i.

3. Try different shapes of the input pulse and record the response of the single channel analyzer.

4. Complete diagram in Fig. 6.4.3 by inserting the observed pulse shapes at the appropriate points.

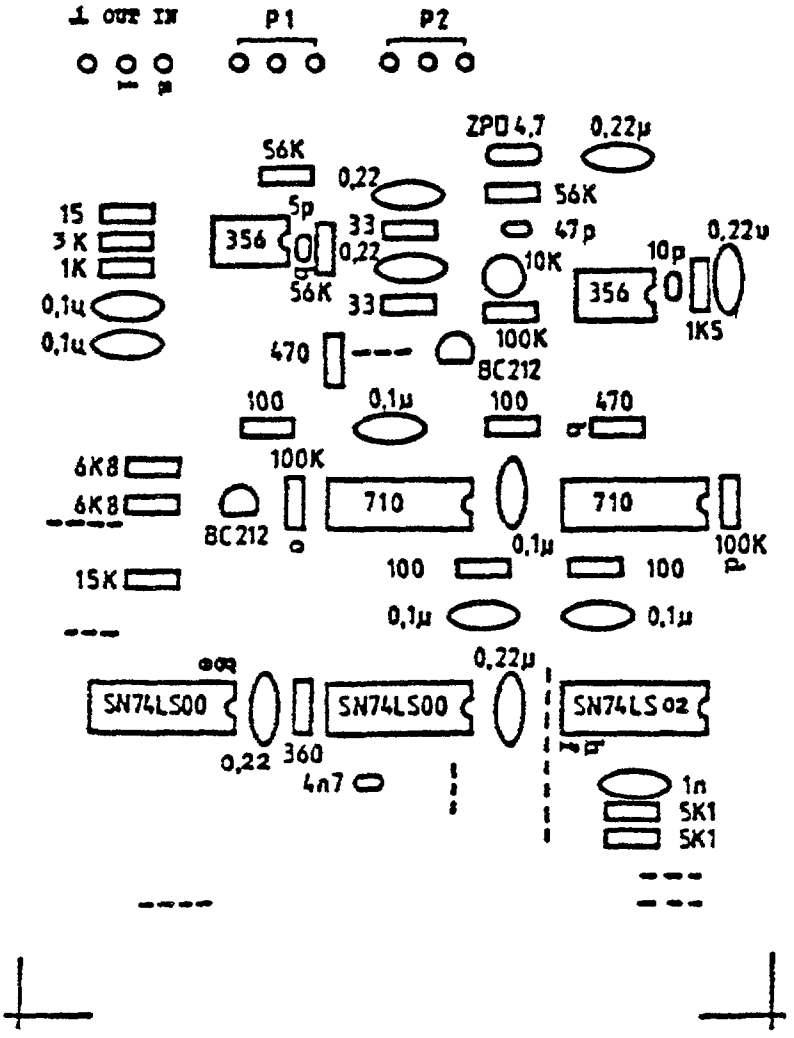


Fig. 6.4.4: SCA component layout;

Notes:

SPECIAL PROJECT 6.5

WILKINSON TYPE CONVERTER

OBJECTIVES

Following the instruction for this experiment, and in combination withe the Special Project 6.6, a complete computer-controlled multichannel analyzer with professional features can be assembled.

REVIEW

The Wilkinson ADC shown in Fig.6.5.1 is the improved version of the analog to digital converter described in the Experiment 4.2. The following improvements were introduced:

1. The described converter is faster. It uses a clock running at a frequency of 30 MHz. Therefore, CMOS circuits which can only operate up to 5 MHz were replaced by their TTL equivalents.

2. The temperature dependant relaxation oscillator used as the clock has been replaced by a more stable crystal controlled oscillator.

3. The crystal controlled clock runs continuously; therefore, synchronization must be introduced. The constant current source discharging the capacitor and the pulse counting should start at clock transitions only.

4. Pulses from nuclear radiation detectors are random in time. A second pulse can arrive before the first one has been analyzed. After a pulse is accepted for analysis, a special circuit disconnects the input until the analysis is completed, eliminating the interference from any following pulses.

5. The saturated transistor input gate is controlled by pulses from the comparator. Faster switching response times have been added (see Experiment 2.14).

6. The output of the input amplifier is buffered by a transistor, allowing a larger current to be used for charging the peak value storing capacitor.

7. For pulses exceeding the full range of the analyzer, the conversion time is longer than 256 x CLOCK PERIOD. After 256 clock periods, the counter starts counting from zero again providing an erroneous result. To avoid the recording of overflow pulses, the OVERFLOW FLIPFLOP is activated. When activated, the end of conversion (EOC) pulse can not be released.

Because of the many new features introduced, the block diagram of the new Wilkinson type ADC is complex (Fig.6.5.1.). Notice the numbering which has been introduced for easier tracking of the signals. Following the signal processing step by step we can observe:

1. Pulse arrives at the input. The input gate is closed because of the conducting Q3, but the pulse arrival is announced by the low level discriminatory LLD.

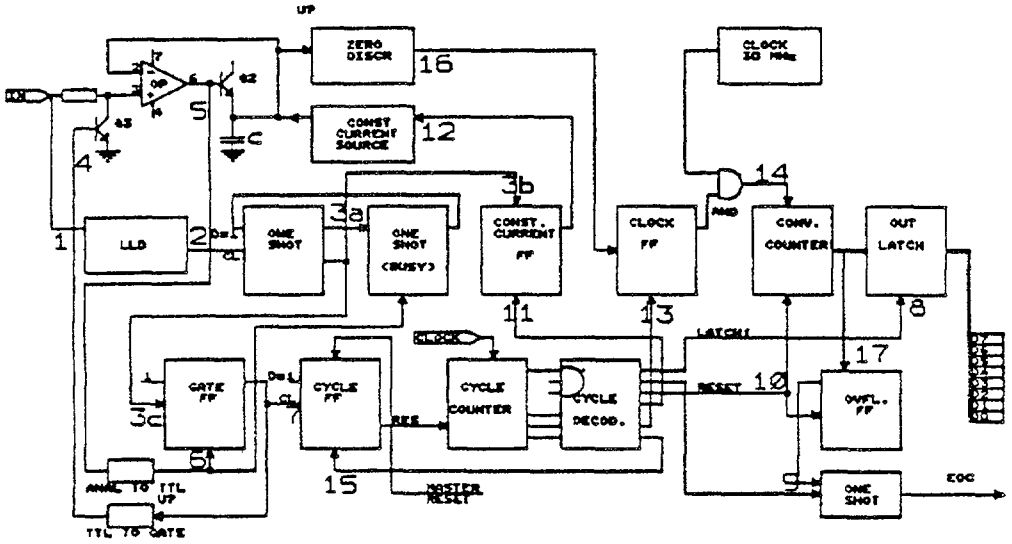


Fig. 6.5.1:

Wilkinson ADC: block diagram.

2. The LLD output activates a ONE SHOT. This one shot is designed using a D-type flipflop with preset and clear. The activation is possible if the D input is in the high state. This is the case when the ADC is not busy. If busy, the analysis procedure is stopped and the pulse will not be converted.

3.

3.a. The resulting pulse at the output of the ONE SHOT will trigger the next ONE SHOT(BUSY). Until the ONE SHOT(BUSY) is activated the path from LLD to ONE SHOT is closed.

3.b. The constant current controlling flipflop CONSTANT CURRENT FF stops discharging the storage capacitor. It is now ready to be charged to the peak value of the incoming pulse.

3.c. The flipflop GATE FF controlling the linear gate is set. Its output signal is transmitted through the fast comparator to the base of the gating transistor.

4. The gating transistor becomes nonconducting and the input pulse is applied to the noninverting input of the amplifier OP; the capacitor C is now being charged. From the triggering of the low level discriminatory until now, all the actions were performed within a few nanoseconds.

5. Now we wait for the message that the peak of the input pulse has been detected. The voltage of the fully charged capacitor C, observed at the noninverting input of (pin 2) of the operational amplifier OP will become less than the voltage at the inverting input (pin 3). Therefore the output of the amplifier will go low. The resulting voltage dropping from few volts to -15V is converted into the voltage suitable for TTL circuits in the ANALOG TO TTL LEVEL shifter.

6. The gate controlling flipflop GATE FF is reset.

7.

7.a. The input transistor gate is closed again.

7.b.The falling edge of the pulse released by the GATE FF activates the CYCLE FF.

The CYCLE COUNTER, kept passive till now because of the permanently applied reset command, is released. It starts to count clock pulses from the CLOCK. CYCLE COUNTER and CYCLE DECODER produces a train of 8 separate pulses. These pulses initiate the next actions.

8. Result of the previous measurement till now kept in the CONVERSION COUNTER is stored in the OUT LATCH.

9. End of conversion pulse is triggered. The computer can take D0-D7 results.

10. CONVERSION COUNTER is reset, as well as the OVERFLOW FLIPFLOP. The ADC is ready to start the new conversion.

11. The constant current controlling flipflop is toggled.

12. The constant current source starts to deliver the current. The voltage across the capacitor C starts to decrease.

13. To avoid the transient effects accompanying the constant current switching, the measurement will start few clock periods later. The Q output of the clock controlling flipflop goes high.

14. The clock pulses are collected in the conversion counter.

15. The cycle defined by the cycle counter is over. The last pulse from the cycle decoder resets the cycle flipflop. The cycle flipflop will remain reset until the next pulse is to be analyzed.

16. The ZERO discriminatory waits until the voltage on the capacitor C reaches zero voltage. (Actually it is set slightly lower. We started counting a few clock periods late. The counting loses are compensated by lowering the transition level of the zero level discriminatory.) The clock flipflop stops counting. The measurement is complete and the ONE SHOT (BUSY) could be released. However, the initial state of the converter has not been restored yet. During the counting, the output voltage of the operational amplifier is saturated negative. When the ZERO discriminatory reaches zero level, the OP should return also be returned to its initial state. However, because of the finite response time, determined by its slew rate, it takes a few hundred of nanoseconds to reach a positive level. The voltage across capacitor C which became negative is now returned to zero; the current from the OP is balanced with the current from the constant current source which is still active.

17. If the input pulse height is greater than the range which can be analyzed, the 8-bit range of the CONVERSION COUNTER will be exceeded. The overflow ninth bit is registered in the OVERFLOW FLIPFLOP. When the conversion is completed (it should not be stopped because we have to discharge the storing capacitor) the ONE SHOT can not be triggered to produce the EOC pulse. If the OVERFLOW FLIPFLOP has been set, the erroneous measurement is not transferred to the computer.

EXPERIMENT

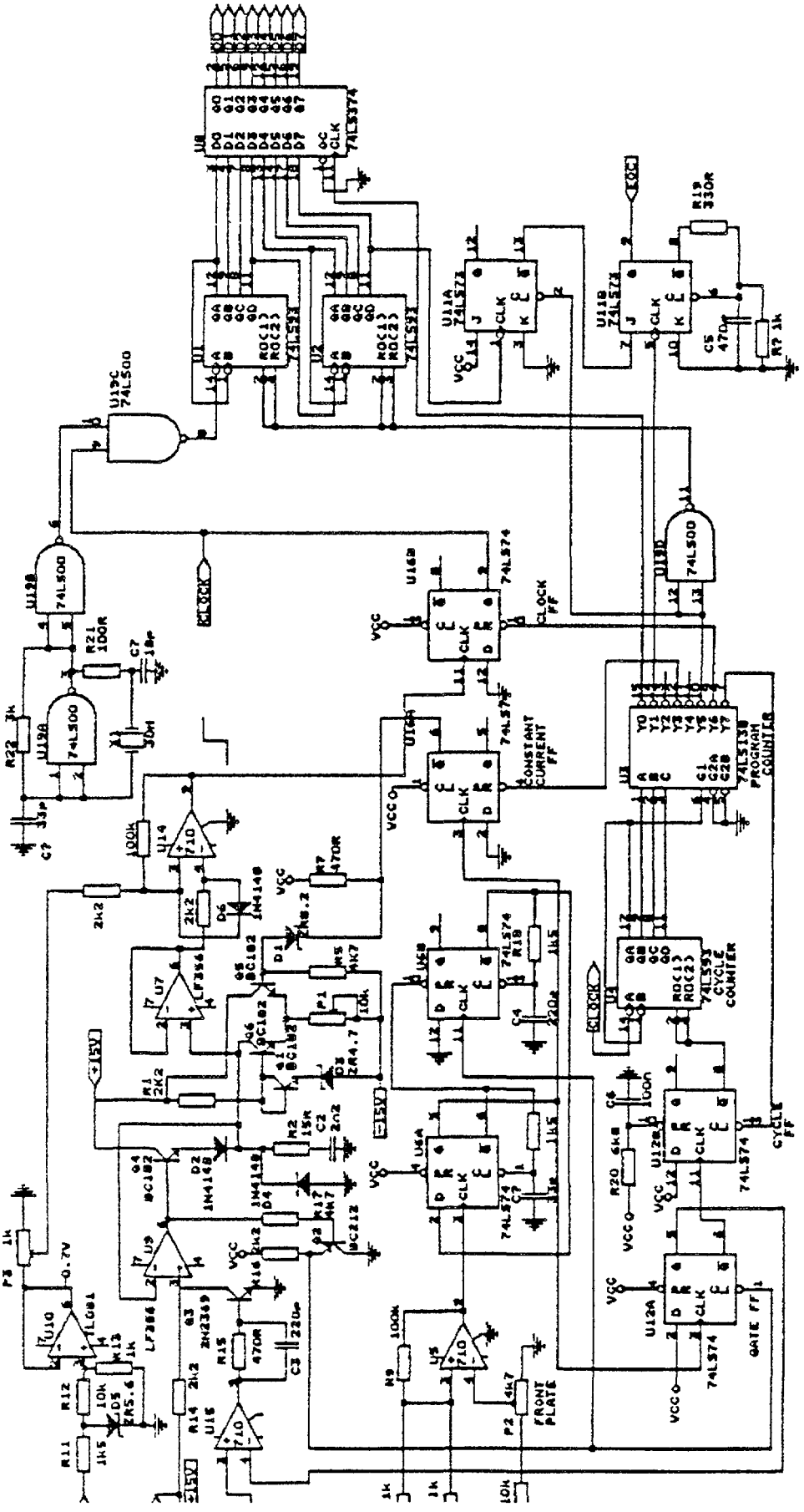
The wiring diagram of the ADC is shown in Fig.6.5.2. You can recognize the separate blocks described in the previous figure. The wiring diagram layout follows the block diagram layout. Note, for easier orientation:

i. The LOW LEVEL discriminatory is U5

ii. The ONE SHOT (BUSY) is U6B

Fig. 6.5.2:

Wilkinson ADC: complete wiring diagram.



iii. The CONVERSION COUNTER is U1 followed by U2.

iv. Between the pulse peak detector (U9) and the ZERO discriminatory, the voltage follower (U7) has been introduced. Because of its high input impedance (LF356) does not load the storing capacitor C2. A LM710 could be used for the ZERO discriminatory LM710; it is fast but takes too much input current.

v. The negative reference voltage used by the ZERO discriminatory is produced by the voltage follower using a TL081 operational amplifier (U10).

vi. Diode D5 clamps the LM710 input voltage which should not exceed 5V (see the corresponding data sheets).

Try to analyze the circuit in all details. A good exercise is to determine how to add the next four bits to achieve 12-bit conversion. The clock frequency should be increased to 100 MHz. Prepare the modified scheme.

Notes:

SPECIAL PROJECT 6.6

ADC COMPUTER LINK

OBJECTIVES

A design for an interfacing unit to connect an external ADC to a computer is preseted. An add-on card for a PC computer will be constructed, with the circuits required to control the data flow and storage.

REVIEW

The function of a MultiChannel Analyzer (MCA) is to count pulses, sorting them according to their height and displaying the resulting spectrum on the screen. The MCAs presently being built feature many additional functions which are built into software rather than the hardware. Plug-in MCAs for the XT/AT type computers are becoming very popular due to the fact that almost everyone has a computer of quite high computational ability; the only thing needed is hardware to collect the data and a program to handle it. By adding these features one gets a far more versatile tool than with a stand alone MCA. And in addition, a computer can be upgraded with new tools to accomplish new tasks.

Let us consider building such an MCA. It will be connected to the computer continuously. It will gather data and the computer will take this data out of it few times per second and store the results in the computer memory. The computer will be responsible for presenting the data on the screen and dealing with the timing. The MCA should be able to handle pulses with rates up to 100 khz without losing any of them. In addition, it should work with up to 12-bit ADCs. The MCA should work regardless of speed of the computer.

Pulses from the detector usually travel through a chain of analog modules such as a preamplifier and amplifier and are finally fed to the Analog to Digital Converter (ADC) (whatever type, whatever speed). This generates a Digital Equivalent of the Pulse Height (DEPH) signal and an additional End Of Conversion (EOC) signal when the DEPH is valid (Fig. 6.6.1).

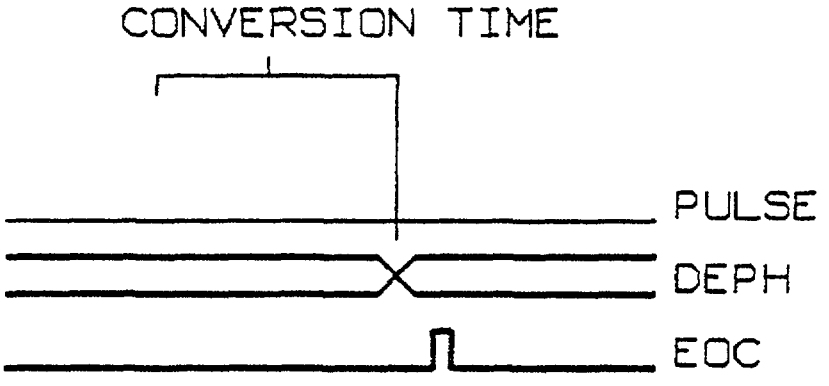
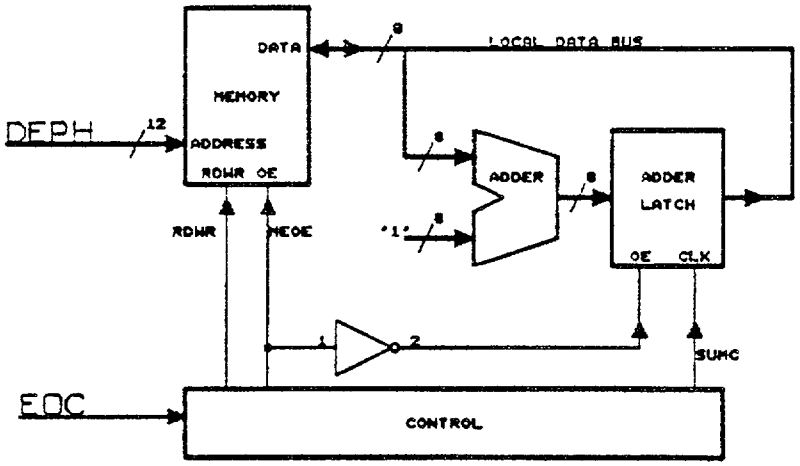


Fig. 6.6.1: Timing digram for analog-to-digital conversion.

The MCA employs a memory to store the number of pulses with the same DEPH. The DEPH word is used as an address and it points to the memory location with the corresponding number of the pulses with equal pulse height. When the EOC signal arrives, the MCA takes the DEPH word, looks at the corresponding memory location for how many pulses of the same height were already registered; increments this value and stores the newly made result back into the memory. A typical block diagram is shown in Fig.6.6.2.

Fig. 6.6.2:

Block diagram of the digital part of MCA: ADD-1 and memory circuit.

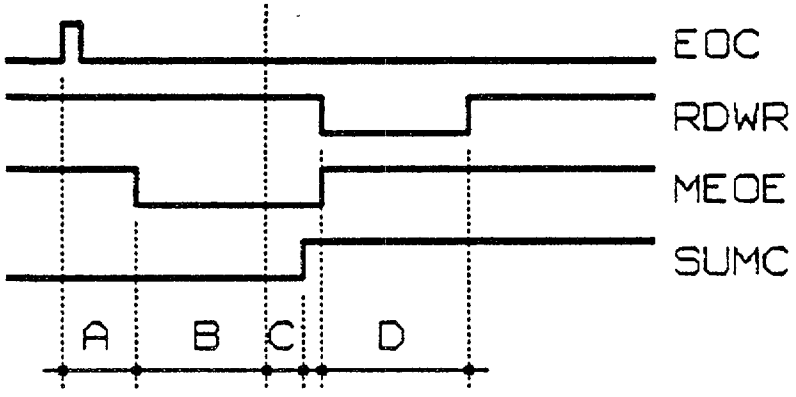


The data at the adder input is valid only during the memory read, so the result of the addition has to be stored in a adder latch prior writing it back to the memory. The control signal, SUMC, does this on its positive going edge.

In order for this kind of a circuit to operate properly, a control circuit has to be employed. As shown, the output of the adder latch and the output data from the memory are connected to the same local data bus. Therefore, they must not be enabled at the same time. The control circuit generates the ReaD/WRite (RDWR) and MEmory Output Enable (MEOE) signals for the memory and adder circuit (Fig.6.6.3).

Fig. 6.6.3:

Timing diagram for for circuit in Fig. 6.6.2.



A: Delay, the circuit needs some time to respond.

B: Memory read, the memory output is enabled and the data is entered on the local data bus.

C: Summation, the data is still available on the local data bus and the sum is being constructed in the adder; this sum is latched into adder latch at the end of this cycle with the SUMC signal.

D: Memory write, the adder latch is enabled to place the result of the summation on the local data bus and this value is written into the memory.

The operation of this circuit is acceptable except for the number of pulses we can store in one channel (one memory location). Eight-bit wide memories are commonly available and, therefore, it is possible to store only 256 events of the same height in one channel. This is not enough.

Let us consider a maximum counting rate of 100000 pulses per second. By transferring the accumulated pulses out of the MCA's memory to the computer twice per second (this value is arbitrarily selected), the memory should be capable of storing 50000 pulses. Assuming that there is just one peak in the spectrum and that a typical peak will be at least three channels wide, one channel has to accumulate 50000/3 or approximately 16000 counts. To store this many counts, a minimum of 14 bits is required. If this is not enough we can move the accumulated data out of the MCA more frequently.

Therefore, two bytes will be needed for storing the data in one channel. With a maximum number of 4k channels this requires 4k x 2 bytes or 8k of 8-bit memory. Memories of this size are cheap and fast enough for the purpose.

By using two byte words, the incrementing sequence gets a bit more complicated. First consider the process of adding two decimal numbers with two digits, for instance 1 and 19.

$$\begin{array}{r} 1 \\ 19 \\ \hline ?? \end{array}$$

The Least Significant Digits (LSD) are added first to make an intermediate sum, that is 1 + 9 = 10. The 0 is used as a LSD result and the 1 is considered to be a carry from the LSD addition to the Most Significant Digit (MSD) addition. So the second addition will add the carry from the first addition to the number 19's MSD. This algorithm can be applied also for other numbers where the carry from the LSD to the MSD doesn't exist.

The same thing happens when adding two bytes. Adding one to the least significant byte is done first. This means reading the low byte out of the memory; incrementing it; storing the result into the adder latch; and writing the contents of the latch back into the memory. After finishing with the low byte, a carry may exist from the low byte to the high byte (it can be stored in a flip-flop); the adder doesn't increment the high byte read out of the memory; it just adds the carry from the previous addition to it. The result of adding the carry is again temporarily stored in the adder latch and a moment later written back into the high byte memory.

The first addition can be simplified. Adding one is exactly the same as adding a carry to a byte. So instead of adding one to the LSD, a carry into the first addition can be set. The whole adding sequence now looks like this:

1. Start the summing cycle.
2. Get the low byte out of the memory and set the carry in to 1.
3. Wait for the sum.

4. Write the low byte sum into the adder latch and store a carry to be input for the high byte addition.
5. Write the sum from the adder latch into the low byte memory.
6. Delay until writing is complete.
7. End of writing the low byte.
8. Read the high byte out of the memory.
9. Wait for high byte.
10. Make a high byte sum (add carry from low byte summation).
11. Write the high byte sum into the adder latch.
12. Write the content of the latch into the high byte memory.
13. Delay until writing is complete.
14. Finish the adding cycle.
15. Release everything.

With the memory used in this experiment, each step in the former sequence takes 0.1 μs; that means the whole adding sequence takes only 1.5 μs. By using a faster version of the memory, it is possible to shorten this time to less than 1 ms (the extra speed is not needed in this case).

The simplest way of adding is to use a Full Adder circuit like the LS83 or an Arithmetic Logic Unit like the LS181. These are all 4 bit units so we would need two of them to work with one byte at a time. Beside these components, we would need a latch to store the addition result during memory write and a special flip-flop to store the carry from the low byte to the high byte addition. In order to reduce the number of chips, let us consider using a PAL device instead and programming all of the necessary logic functions for addition into it.

A GAL device can act exactly the same as a PAL but it can be reprogrammed. This is a great benefit for us, allowing us to change our minds during development. Once the development is complete we can keep the programmed GAL device or program a PAL to do the same thing for us (PAL's are a bit cheaper, but this counts only in production quantities). The programming of the device is done with the CUPL program and the device itself is programmed on a XT/AT plug-in programming unit.

Let us consider adding the carry (COUT, this may be '0' or '1') and one byte of data. The input byte of data consists of bits marked MD0 for the least significant bit to MD6 for the most significant bit. The output byte of data is marked MDO0 to MDO6. It is only seven bits long; the reason will be explained later.

							COUT
+	MD6	MD5	MD4	MD3	MD2	MD1	MD0
	MDO6	MDO5	MDO4	MDO3	MDO2	MDO1	MDO0

Let us first consider how to add the least significant bit. MDO0 will be high if MD0 is high and COUT is low or if MD0 is low and COUT is high. Therefore:

```
MDO0 = MD0 & !COUT # !MD0 & COUT; where
```

! stands for NOT (inversion) in CUPL
& stands for AND in CUPL
# stands for OR in CUPL

Similarly the MDO1 will be high if:
- MD1 is high and MD0 is low and COUT is low or
- MD1 is high and MD0 is low and COUT is high or
- MD1 is high and MD0 is high and COUT is low or
- MD1 is low and MD0 is high and COUT is high

This can be written as:

```
MDO1 = MD1 & !MD0 & !COUT #
       MD1 & !MD0 &  COUT #
       MD1 &  MD0 & !COUT #
       !MD1 &  MD0 &  COUT;
```

The first two lines of the equation can be reduced to:

```
MDO1 = MD1 & !MD0 #
       MD1 &  MD0 & !COUT #
       !MD1 &  MD0 &  COUT;
```

The equations for the rest of the bits can be similarly written. The last equation stands for carry out signal: it is high when all of the bits MD0 to MD6 are high and the COUT signal is high. At the beginning of the addition cycle at stage 2, the COUT signal should be set with the SCIN signal (setting a carry into an addition is the same as adding one) therefore the equation for COUT looks like:

```
COUT = MD6 & MD5 & MD4 & MD3 & MD2 & MD1 & MD0 & COUT #
       SCIN.
```

As previously mentioned, there are only 7 bits per byte. There are only 8 outputs with GAL device. One of them has to be used for COUT signal so only seven of them remain for the data. Two bytes each with seven bits of data gives 14 bits which is sufficient for our needs.

The result of the addition with the calculated carry will be written to the latch in the GAL internal logic with the rising edge of the SUMC signal. Because the equations written so far actually represent signals connected to the inputs of these latches (they are D type flip-flops), the grammatics in CUPL will specify these inputs by appending a .D after the name of signal connected there.

One additional signal called ADDR is needed to control the adding sequence. This controls one of the address lines of the memory. During the first part of the addition cycle, the low part (seven bits now) of the word is read out and then written back into the memory; later the high part is processed. The control signals sequence for adding is given in Fig .6.6.4. The dashed lines represent the boundaries between the states. The MODE, L1CL, and L2CL signals will be mentioned latter.

Let us now continue looking at the summing sequence. This sequence refers to the block diagram on Fig. 6.6.5. If the MCA is busy with a sequence then it finishes the sequence first. If the MCA is not busy (it is in an initial state) and there is nothing to be done then it stays ready to accept data. If the MCA is not busy but an EOC signal was activated then adding cycle has been started and this cycle will be completed regardless of the state at the inputs.

Fig. 6.6.4:

Adding sequance for 32 k/channel range,

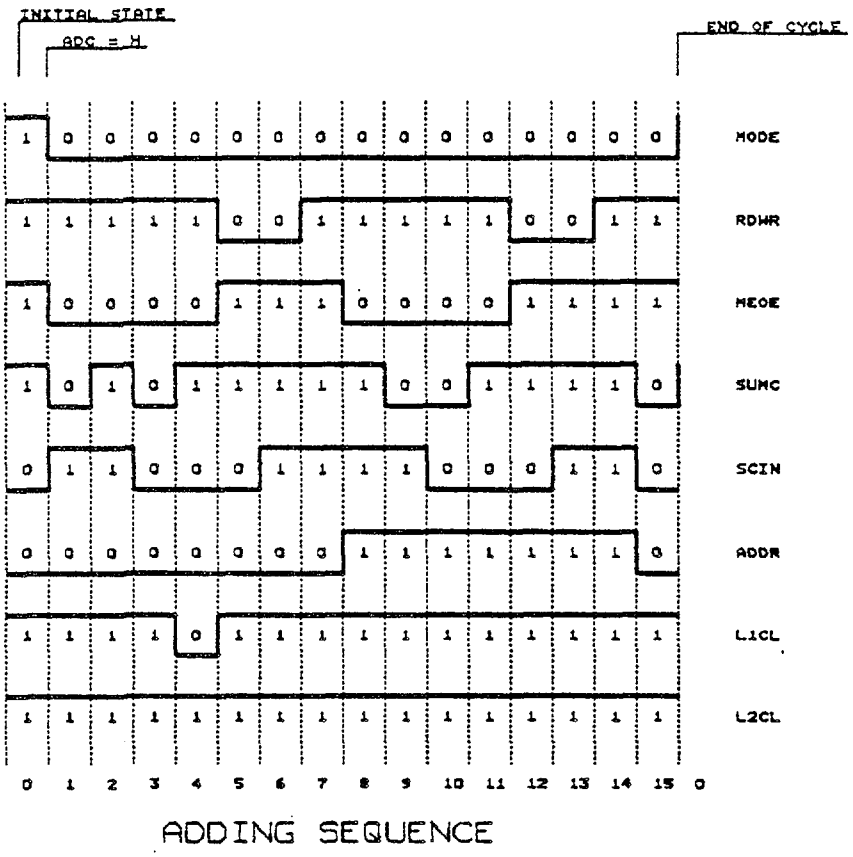
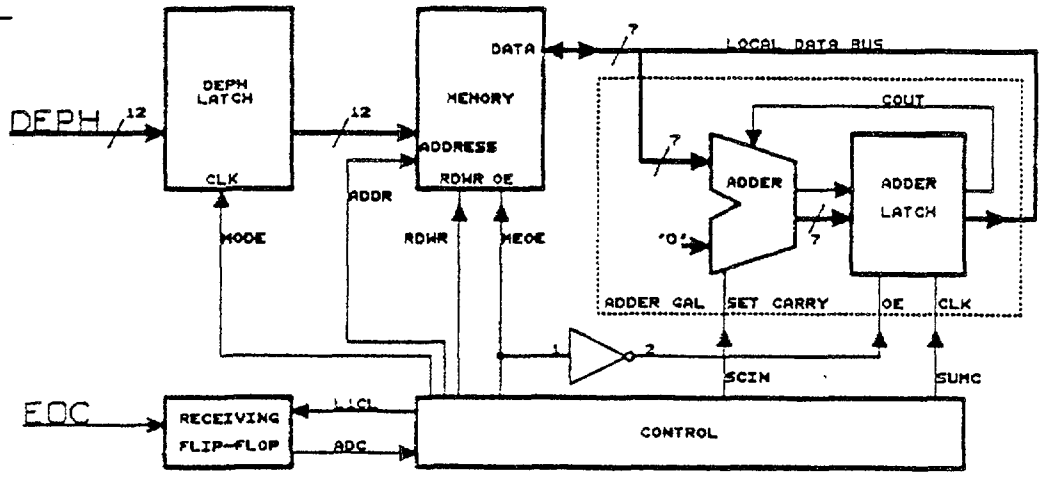


Fig. 6.6.5:

Block diagram of ADD-1 and memory circuit using GAL.



The summing sequence is as follows:

1. MEmory Output Enable (MEOE) goes low so the contents of the memory location given by DEPH is loaded onto the local data bus.

The RDWR signal remains high; this means the read from memory, SCIN, signal goes high so the carry will be set to go high during the next SUMC positive edge.

The ADDR signal remains low to select the low byte to be worked on.

2. The fact that the SCIN signal is high is written into the adder latch on the rising edge of the SUMC signal; everything is now ready for incrementing the word that will come out of the memory after the memory access time (200ns at most).

3. The low byte is available at the data bus and during this state it is incremented in the GAL device. The SCIN signal goes low so as to not be written into the adder latch during next SCIN rising edge.

4. On the SUMC rising edge the result of the increment is written into the adder latch, together with the carry to the high byte (this will be taken care of during next stage).

5. The MEOE signal disables the memory output and activates the adder latch outputs, placing the result of the addition on the local data bus.

The RDWR signal goes low to write the content of the local data bus into the memory.

6. Writing into memory takes 200 ns at most, so this stage is required only to wait for specified delay time.

7. When the writing into the memory is complete, the RDWR signal goes high, low byte is done and the carry exists in the latch.

8. The ADDR line goes high, signaling the memory that high byte is now to be processed. The MEOE signal goes low and the contents of the high byte of the memory is loaded onto the local data bus.

9. Delay while waiting for the high byte to be loaded (200ns max).

10. The high byte is now available on the local data bus and the sum is being constructed in SUM GAL device. The SCIN signal goes low to prevent the carry from being set during next rising SUMC edge (not important).

11. On the SUMC rising edge the result of the addition is written into the adder latch.

12. The MEOE signal disables the memory output and enables the adder latch to place the result of the addition on the local data bus. The RDWR signal goes low to write the contents of the local data bus into the memory.

13. Delay while writing into memory (200 ns at most).

14. The RDWR signal goes high again to end the writing.

15. The end of cycle; all of the signals reset back to the initial state.

Every incoming DEPH information signal accompanied by the EOC signal will, therefore, add one to the corresponding word in memory. After a sufficient number of pulses have been recorded, there is a spectrum available in the MCA memory.

With the circuit described, the DEPH must not change during the addition process. If it does (and it is possible due to the random nature of the incoming pulses) the addition is

faulted. It is a good idea to latch the DEPH immediately after starting an adding sequence. For this, one additional signal is needed to control the latch; let us call it MODE. It goes low in stage 1 to latch the DEPH during adding sequence and high again in stage 15 to release the latch (Fig.6.6.4 and Fig 6.6.5).

One additional flip-flop is required to receive the EOC signal. It may happen that the MCA is busy with the previous pulse or with sending data to the computer when a new pulse arrives. Therefore, the EOC signal activates a flip-flop with the ADC signal alerting the control circuit to do something. When the control circuit is ready to handle the incoming pulse, it starts an adding sequence which can not be interrupted. The DEPH data is immediately latched. During stage 4, the receiving flip-flop is cleared with the L1CL signal and from then on it is ready to store the next EOC signal. Therefore, if two pulses (two EOC signals) come as close as 500ns (every state leasts 100ns), they will be still recorded properly. In this case there must be at least one adding cycle (1.5μs) of free time to allow the MCA to store the pulses. If this is not the case then one pulse will be lost.

Having a spectrum stored in the MCA memory is a nice achievement but it is worthless unless the data can be presented to the user. Therefore there must be some means of transferring the collected data to the computer. The computer can then draw the spectrum on the screen and make all the required calculations. The simplest solution to the problem seems to be to have two memories. While one of them collecting data the other is available to the computer and vice versa. In this case a large multiplexer is required. All of the address, data and control lines of the memory have to be switched between two sources and two destinations. to complicate things further, some of the lines are bidirectional. So this is not the wisest solution.

We have assumed a maximum pulse rate of 100 kHz; that is 10 μs between pulses. Therefore, there should be between the incoming pulses to take data out of the MCA. Since storing a pulse only takes 1.5 us, 8.5 us should be available for the computer. This is partially true. Due to the random nature of the incoming pulses, the spacing may differ from this average value.

Storing the data coming from the ADC has absolute priority. The computer can wait; the experiment can not. The computer is a rather slow device, especially the old 4.77 MHz XT units. Therefore, it is better not to rely on the computer's ability to take data out of the MCA but to allow the computer just to ask MCA to prepare data for it. The computer can execute an idle loop until the data is ready to be moved.

The data will be moved to the computer channel by channel; the computer will supply only the requested channel number (memory address) and a request signal to the MCA to prepare data. This request signal can be simply a write signal for the channel number. The computer can store the channel number in an address latch where it will wait for the MCA to take it. When MCA is not busy it will take this address out of the address latch and read the memory contents (two seven bit bytes). It will then place the contents into an intermediate latch until the computer can take it. After the data has been moved to the latch the contents of the MCA memory at this address are zeroed.

The whole transfer sequence from the computer side looks like this:

A. Send channel number to the MCA

B. Wait until MCA signals the data is ready

C. Read data from the MCA

From the MCA side (when it is free, that is not busy with an addition cycle or previous transfer cycle):

1. Start transfer cycle active.
2. Read low byte out of the memory (seven bits), using the address stored in the address latch.
3. Delay until the memory read is complete.
4. Store contents of the low byte of the memory into the low byte intermediate latch.
5. Write zero in the memory at low byte location.
6. Delay until the memory write is complete.
7. Finish first writing.
8. Read the high byte out of the memory (seven bits only); use the address stored in the address latch.
9. Delay until the memory read is complete.
10. Store the contents of the high byte of memory into the high byte intermediate latch.
11. Wait.
12. Write zero into the memory at high byte location.
13. Delay until the memory write is complete.
14. Finish second writing.
15. Release and reset everything.

This sequence looks very similar to the former adding sequence except for writing zero back into the memory instead of writing the sum and the two extra writes into the intermediate latch (Fig. 6.6.6).

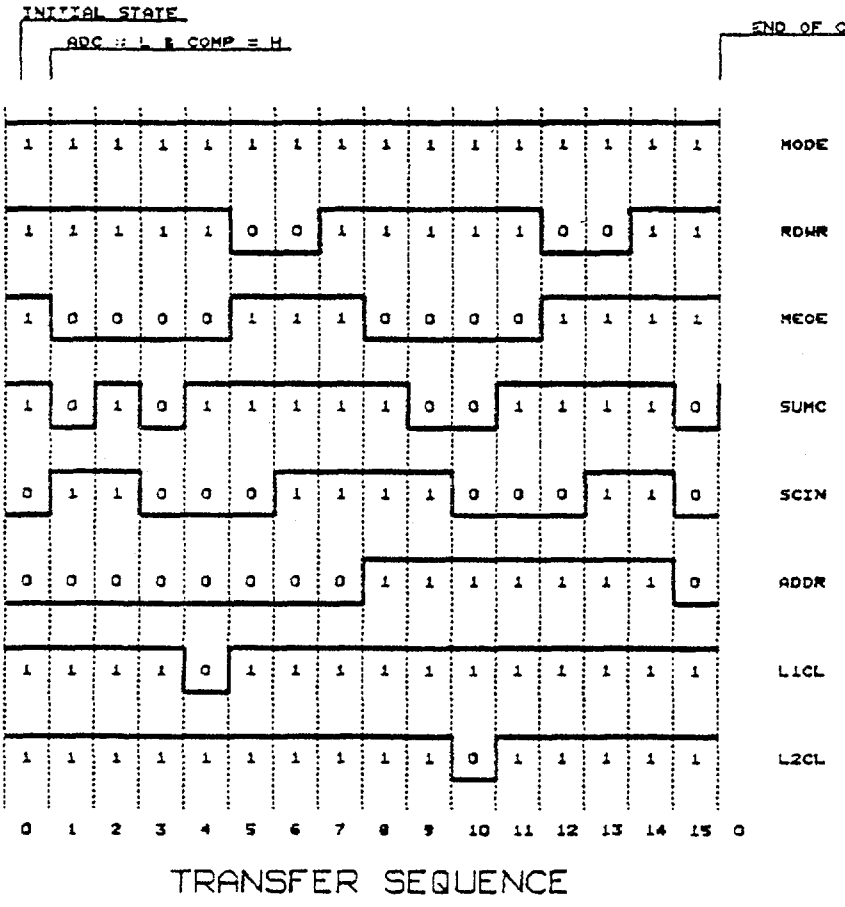


Fig. 6.6.6: Transfer sequence

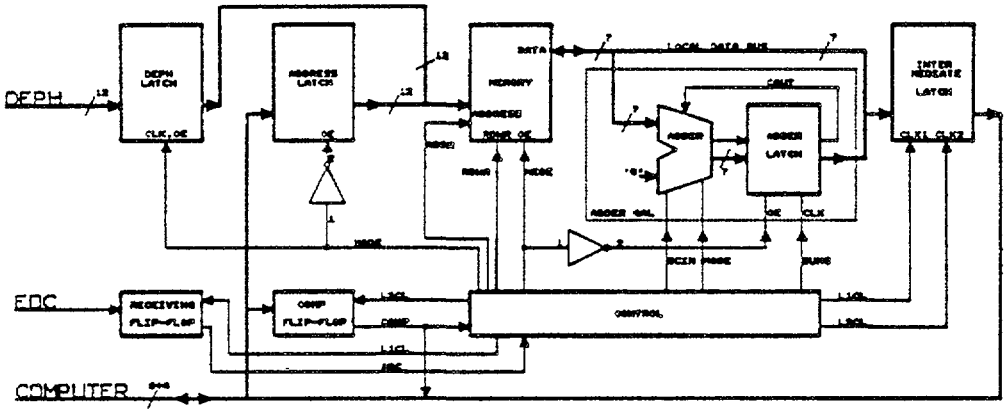
Zeroing the memory is easy. The MODE signal is low only during the adding sequence. By modifying the equations in SUM GAL device to make a sum only when the MODE signal is low and producing zero at the outputs when the MODE signal is high the problem is solved.

Writing into the intermediate latch must occur immediately after reading the contents of the memory. The L1CL signal is quite suitable for this purpose. It has to write data from the local data bus only in the case of a transfer cycle, so it has to be combined with the MODE signal. For writing the high byte an additional L2CL signal has to be generated. It takes place in stage 10, when the second byte is available at the local data bus (Fig.6.6.6).

The channel number requested by the computer is stored in an address latch and also the DEPH is latched. The latches have three output states. There is already a MODE signal and it is low only during the adding sequence when the DEPH latch has to be connected to the memory. It is possible to use the MODE signal to select either the DEPH latch during adding sequence or the address latch during the transfer sequence to supply the address for the memory (Fig. 6.6.7).

Fig. 6.6.7:

Block diagram of the ADC-computer link.



There is an additional flip-flop shown on the diagram. The computer may ask the MCA to prepare data while the MCA is busy. That is why the computer request is stored in a flip-flop (COMP) similar to the EOC signal and stays there until the MCA finishes the transfer cycle. The L2CL signal ends the cycle and it also clears this flip-flop. The computer has to wait until the contents of the memory location is written into the intermediate latch. It waits until the COMP signal is high. Therefore, this signal is also available to the computer.

Let us continue studying the transfer cycle.

If the MCA is busy, it will finish the current cycle. If the MCA is free and there is nothing to be done (no flip-flops set) it will stay free (in initial state). If the MCA is free and an EOC signal has been received then it will do the adding cycle. If the MCA is free and only a computer request was received then it will do the transfer cycle.

1. The MODE signal stays high during the transfer cycle.

The MEOE goes low; RDWR stays high; the contents of the memory specified by the address latch and the ADDR signal is loaded onto the local data bus.

2. Delay while reading the memory (200ns max).

3. Still waiting.

4. On falling edge of the L1CL signal, the data available on the local data bus is written into the low byte intermediate latch.

On rising edge of the SUMC signal, zeroes are written into the adder latch (the MODE signal is high, does not do addition; see the SUM GAL equations).

5. The MEOE signal goes high disabling the memory from the local data bus and enables the adder to place zeroes on the local data bus.

When the RDWR signal goes low the contents of the local data bus are written into the memory location specified by the address latch and the ADDR signal.

6. Delay until the memory write is completed.

7. The RDWR signal goes high; the end of writing.

8. The ADDR changes to high; the high byte is to be processed.

The MEOE signal goes low again requesting the high byte to be transferred to the local data bus.

9. Delay while reading.

10. Still waiting, but prepare the L2CL signal.

11. On rising edge of the L2CL signal, the contents of the local data bus are stored into the high byte the intermediate latch.

Both bytes are now available at the intermediate latch so the requesting flip-flop (COMP) can also be cleared with the L2CL.

12. the MEOE signal goes high disconnecting the memory from the local data bus and enabling the adder to place zeroes on the local data bus.

The RDWR signal goes low and the contents of the local data bus are written into the memory location specified by the address latch and the ADDR signal.

13. Delay until the writing is completed.

14. The RDWR signal goes high, the writing is complete.

15. End of the transfer cycle.

The L1CL signal is also used to clear the ADC flip-flop but it is active during both cycles. That is why it has to be combined with the MODE signal to clear the ADC flip-flop only during the adding cycle. This can be seen on the final schematic diagram.

Let us not forget that the computer reads two bytes with eight bits, but the MCA supplies only seven bits of data per byte. One of two spare bits can be used to signal the computer about the data being ready. Bit 7 of the high byte intermediate latch is not connected to the computer data bus. Instead, an additional three state buffer is added to place the COMP signal there. Bit 7 of the low byte intermediate latch is always low. If high byte read out of the MCA by the computer is larger than 127 (bit 7 is high) then the word read is not ready yet and the computer has to read it again. It continues to read it as long as it is not less than or equal to 127. The program for reading out the content of one channel looks like this:

aa: send a channel number to the MCA.

ab: read the contents of the intermediate latch.

ac: if contents of the high byte 127 then goto ab.

ad: rearrange the two seven bit bytes into one 14 bit word.

This procedure has to be repeated for all the channels approximately twice per second. It obvious that the procedure has to be very fast otherwise there will be no time left for the computer to draw the results on the screen. The procedure will have to be written in assembly language. The procedure takes about 3 ms for 256 channels on a 10M Hz AT type computer. This is negligible compared to the 500 ms between data transfers and the data transfers could occur even twice as frequently to allow input pulse rates up to 200 khz with the same number of channels. With more channels it takes linearly longer but in that case fewer pulses are accumulated in a channel (channel is narrower) and transferring data twice per second suffices.

The interface to the computer is made through a unit called the Slot Buffer (described elsewhere). It is only an address and data bus buffer with partially decoded addresses. The function of this unit is to prevent possible damage to the computer by misuse of the MCA. The addresses through which the computer can access the MCA are 300H to 303H and are decoded with a dual 1 of 4 decoder (see the final schematic diagram). They are assigned as follows:

in 302Hlow byte intermediate latch.
in 303Hhigh byte intermediate latch.
out 300Hclear DOIT flip-flop.
out 301Hpreset DOIT flip-flop.
out 302Hlow byte address latch.
out 303Hhigh byte address latch.

It must be possible to control the data gathering process with the computer. It has to be possible to start or stop the process by a software command. This can be done by adding the flip-flop DOIT. By clearing the DOIT flip-flop, the EOC receiving flip-flop is permanently cleared and the gathering of the incoming pulses is disabled. By presetting the DOIT flip-flop, gathering is enabled. Through the DOIT flip-flop the computer can enable or disable the gathering of the data and introduce a preset measuring time. The connection to the circuit can be seen in the last schematic.

Almost everything is now complete except for the control circuit. As seen from the requests, it has to be a state machine (every decision logic produces spikes and can not be used here) consisting of eight flip-flops (eight control signals needed) and a logic circuitry to make these flip-flops follow a required sequence. It runs at 10MHz clock, producing a stage interval of 100ns. It has two inputs, ADC and COMP, for the attention requesting flip-flops. All the necessary logic can be programmed in one single GAL device.

It is possible to connect ADC with less than 12 bits to this MCA. In this case the DEPH lines not used, default to high and the spectrum will, therefore, be stored in the high part of the memory. For an 8-bit ADC this gives addresses 1000H-100H to 1000H (1000H being the last available MCA address). This is important only when writing software for moving data out of the MCA.

Integrated circuit functions:

- U1: DEPH high byte latch
- U2: DEPH low byte latch
- U3: address high byte latch
- U4: address low byte latch

- U5: memory
- U6: intermediate low byte latch
- U7: intermediate high byte latch
- U8: SUM GAL
- U9A: COMP flip-flop
- U9B: EOC receiving flip-flop
- U10: control circuit
- U11A,B: 10MHz oscillator
- U11C: MEOE inverter
- U12A,B: L1CL, MODE and DOIT combining circuit
- U12C: MODE inverter
- U12D: L1CL, MODE combining circuit
- U13: computer address decoder
- U14B: DOIT latch
- U15: COMP three state buffer

The input to the CUPL programme, with the data relevant for the ADC-computer link, is presented in Pages 299-303. For additional infomation on the software tools see Experiment 3.3.

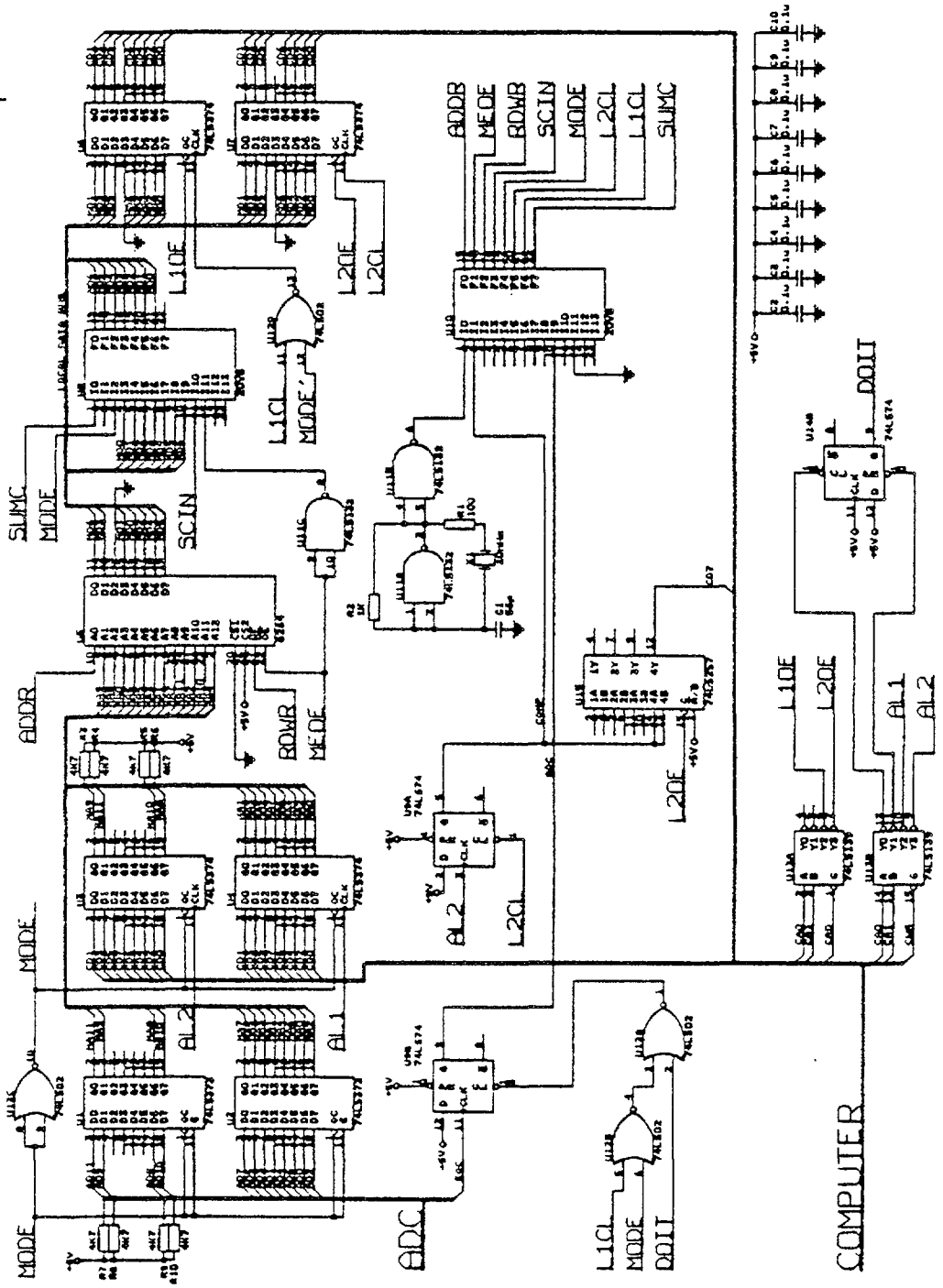


Fig. 6.6.8:

Wiring diagram of the ADC-computer link.

```
;MCA control GAL equations

Name            MCA SEQUENCER;
Partno          002;
Revision        01;
Date            02/06/89;
Designer        DUSAN PONIKVAR;
Company         VTO Fizika;
Location        U6;
Assembly        MCA LOGIC;
Device          G20V8;

Pin 22 = MODE;
Pin 21 = RDWR;
Pin 20 = MEOE;
Pin 19 = SUMC;
Pin 18 = SCIN;
Pin 17 = ADDR;
Pin 16 = L1CL;
Pin 15 = L2CL;

Pin  2 = COMP;
Pin  3 = ADC;
Pin  1 = CLK;


 MODE.D = !RDWR & !MEOE #
           MODE & !MEOE #
           MEOE & !SUMC #
          !ADC  &  RDWR &  MEOE &  SUMC & !SCIN #
          !ADC  &  MODE #
           ADC  &  MODE & !RDWR #
           MODE &  SCIN #
           RDWR &  MEOE &  SUMC & !SCIN &  ADDR;

 RDWR.D = !SUMC #
           RDWR &  MEOE #
           SUMC &  SCIN #
          !RDWR & !MEOE;

 MEOE.D = !RDWR #
          !MEOE &  SUMC & !SCIN #
           MEOE &  ADDR #
           MEOE & !SUMC #
          !ADC  & !COMP &  SUMC & !SCIN;

 SUMC.D = !RDWR #
           MEOE & !SUMC #
          !MEOE & !SCIN #
          !SUMC &  SCIN & !ADDR #
           MEOE &  SUMC &  SCIN & !ADDR #
           SUMC & !SCIN &  ADDR #
          !ADC  & !COMP &  SUMC & !SCIN;

!SCIN.D =  MEOE & !SUMC #
          !MEOE & !RDWR #
          !MEOE &  SUMC & !SCIN #
           RDWR &  MEOE &  ADDR #
          !ADC  & !COMP &  RDWR &  SUMC & !SCIN #
          !SUMC & !SCIN #
```

Fig. 6.6.9: Listing for GAL programming (Part 1).

Fig. 6.6.9:

(cont.)

```
                !SUMC &  SCIN &  ADDR #
                !MEOE &  SUMC &  SCIN & !ADDR;
!ADDR.D =  MEOE & !SUMC #
          !MEOE &  SCIN & !ADDR #
          !SCIN & !ADDR #
          !RDWR & !MEOE #
           RDWR &  MEOE &  ADDR #
          !RDWR & !ADDR;

 L1CL.D =  MEOE #
           ADDR #
           SCIN #
           SUMC #
          !RDWR;

 L2CL.D = !SCIN #
           MEOE #
           SUMC #
          !ADDR #
          !RDWR #
          !MODE;
```

Fig. 6.6.10: Listing for GAL programming (Part II).

```
; SUM GAL equations, CUPL format

Name            MCA_SUMM;
Partno          001;
Revision        01;
Date            03/06/89;
Designer        DUSAN PONIKVAR;
Company         VTO Fizika;
Location        U5;
Assembly        MCA LOGIC;
Device          G20V8;
Format          JEDEC;

Pin 22 = COUT;
Pin 21 = MDO6;
Pin 20 = MDO5;
Pin 19 = MDO4;
Pin 18 = MDO3;
Pin 17 = MDO2;
Pin 16 = MDO1;
Pin 15 = MDO0;

Pin  2 = MODE;
Pin  3 = SCIN;
Pin  4 = MD6;
Pin  5 = MD5;
Pin  6 = MD4;
Pin  7 = MD3;
Pin  8 = MD2;
Pin  9 = MD1;
Pin 10 = MD0;

Pin  1 = SUMC;
Pin 13 = SUOE;


MDO0.D = !MODE &  MD0 & !COUT #
         !MODE & !MD0 &  COUT ;

MDO1.D = !MODE &  MD1 & !MD0 #
         !MODE &  MD1 &  MD0 & !COUT #
         !MODE & !MD1 &  MD0 &  COUT ;

MDO2.D = !MODE &  MD2 & !MD1 #
         !MODE &  MD2 &  MD1 & !MD0 #
         !MODE &  MD2 &  MD1 &  MD0 & !COUT #
         !MODE & !MD2 &  MD1 &  MD0 &  COUT ;

MDO3.D = !MODE &  MD3 & !MD2 #
         !MODE &  MD3 &  MD2 & !MD1 #
         !MODE &  MD3 &  MD2 &  MD1 & !MD0 #
         !MODE &  MD3 &  MD2 &  MD1 &  MD0 & !COUT #
         !MODE & !MD3 &  MD2 &  MD1 &  MD0 &  COUT ;

MDO4.D = !MODE &  MD4 & !MD3 #
         !MODE &  MD4 &  MD3 & !MD2 #
         !MODE &  MD4 &  MD3 &  MD2 & !MD1 #
         !MODE &  MD4 &  MD3 &  MD2 &  MD1 & !MD0 #
         !MODE &  MD4 &  MD3 &  MD2 &  MD1 &  MD0 & !COUT #
```

Fig. 6.6.10:

(cont.)

```
                !MODE & !MD4 &  MD3 &  MD2 &  MD1 &  MD0 &  COUT ;

MDO5.D =  !MODE &  MD5 & !MD4 #
          !MODE &  MD5 &  MD4 & !MD3 #
          !MODE &  MD5 &  MD4 &  MD3 & !MD2 #
          !MODE &  MD5 &  MD4 &  MD3 &  MD2 & !MD1 #
          !MODE &  MD5 &  MD4 &  MD3 &  MD2 &  MD1 & !MD0 #
          !MODE &  MD5 &  MD4 &  MD3 &  MD2 &  MD1 &  MD0 &
          !COUT #
          !MODE & !MD5 &  MD4 &  MD3 &  MD2 &  MD1 &  MD0 &
           COUT ;

MDO6.D =  !MODE &  MD6 & !MD5 #
          !MODE &  MD6 &  MD5 & !MD4 #
          !MODE &  MD6 &  MD5 &  MD4 & !MD3 #
          !MODE &  MD6 &  MD5 &  MD4 &  MD3 & !MD2 #
          !MODE &  MD6 &  MD5 &  MD4 &  MD3 &  MD2 & !MD1 #
          !MODE &  MD6 &  MD5 &  MD4 &  MD3 &  MD2 &  MD1 &
           !MD0 #
          !MODE &  MD6 &  MD5 &  MD4 &  MD3 &  MD2 &  MD1 &
            MD0 & !COUT #
          !MODE & !MD6 &  MD5 &  MD4 &  MD3 &  MD2 &  MD1 &
            MD0 &  COUT ;

COUT.D =  !MODE &  MD6 &  MD5 &  MD4 &  MD3 &  MD2 &  MD1 &
            MD0 &  COUT #
           SCIN ;
```

SPECIAL PROJECT 6.7

STAIRCASE GENERATOR

The objective of this project is to design and build a staircase generator able to serve as a test instrument for base restoration circuitry in nuclear pulse amplifiers.

OBJECTIVES

Base line restorers are essential elements in nuclear amplifiers designed for high resolution spectroscopy. However, it is difficult to ascertain their performance using signals coming either from a detector or from the usual pulse generators. A fast and sensitive test procedure is to apply a train of staircase-like pulses at the amplifier input. The steps should be reasonably flat, but the essential characteristic for the intended application is to have a monotonic progression of the staircase amplitude. Such a characteristic is automatically ensured in the present design, where the steps are obtained by successive addition of independent current sources.

REVIEW

Circuit description

The functional block diagram of the staircase generator is shown in Fig. 6.7.1; the main components related to each block are indicated. The digital part of the generator is designed as a synchronous digital system. The clock advances the system through its various states; the duration of each staircase step is equal to one clock period. The analog staircase voltage is obtained by summing 8 independent currents of identical intensity in a current-to-voltage converter. The current sources are simply resistors connected to Vss through a switch (the other terminal of the resistors is connected to the virtual ground of the summing circuit). The current switch control successively switches on the various current sources, and then switches them off simultaneously. The duty cycle control determines the number of clock cycles during which all current sources are off.

EXPERIMENT

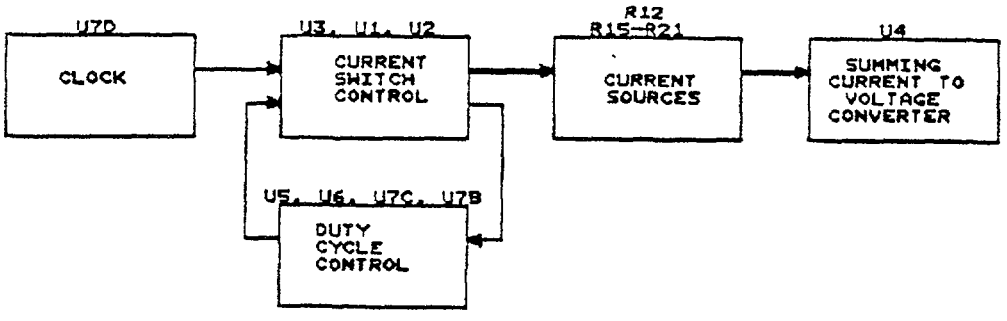


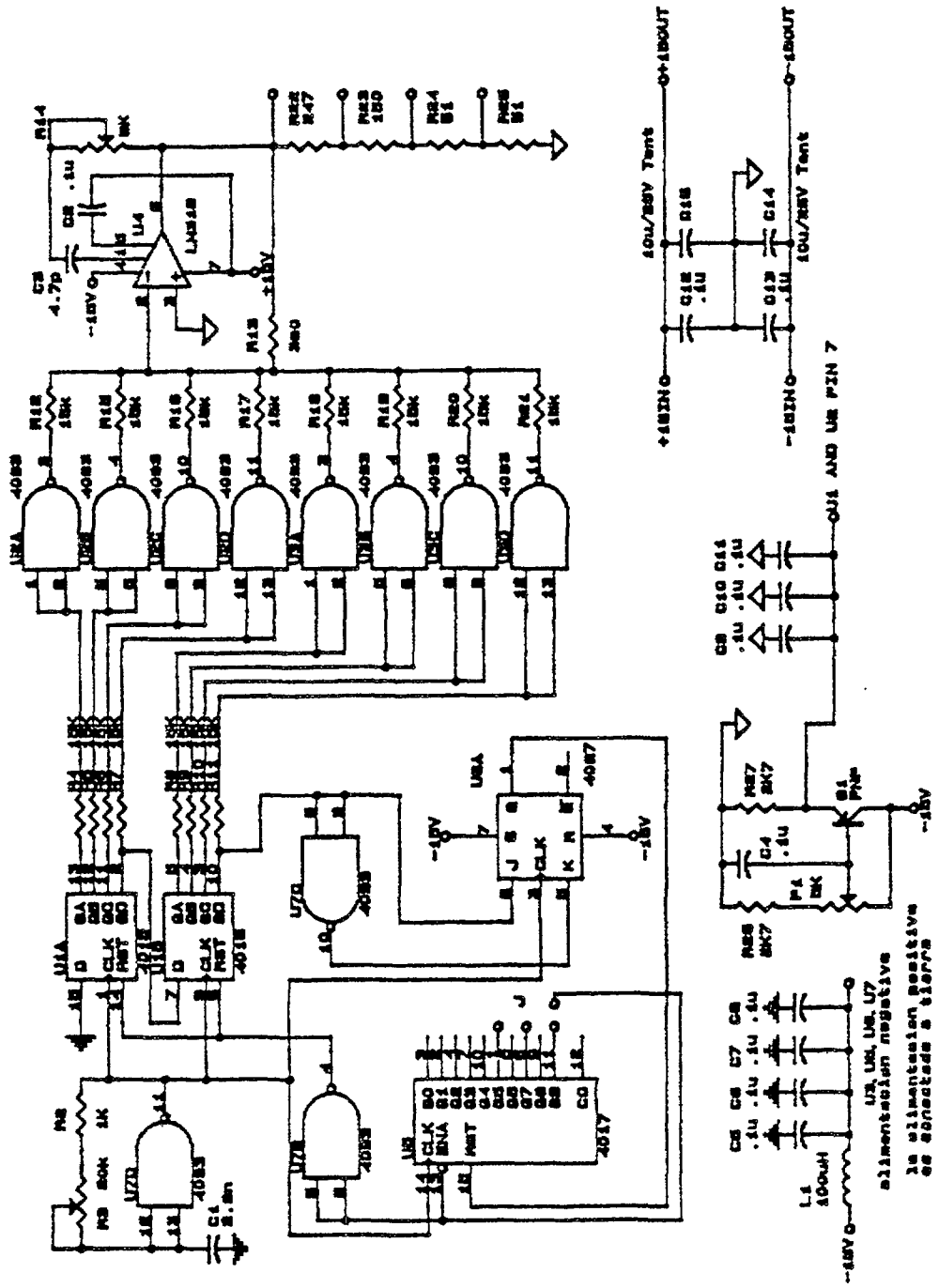
Fig. 6.7.1: Block diagram of staircase generator.

We now describe the detailed circuit diagram of Fig. 6.7.2.

Current summing is obtained in an LM318 operational amplifier in the inverting connection. Lead-lag compensation through C3-R14 is used to increase amplifier stability. Step

Fig. 6.7.2:

Staircase generator wiring diagram.



rise times of about 50 ns have been measured in the prototype circuit. The output voltage signal is made available through a voltage divider, the lower tap of which reduces the output signal by a factor of 1/10.

Each current source is just a 15K resistor connected to the output of a NAND gate of the CD4093 package. This package is powered between V_{DD} at ground and V_{SS} at a negative voltage. This voltage, supplied by Q1, may be varied continuously from roughly -14.3 V to -9 V with potentiometer P1. The current supplied by each current source may thus be continuously adjusted from roughly -1 mA to -0.6 mA. With the 390R amplifier feedback resistor, each current source contributes a step adjustable between approximately 0.39 V and 0.24 V to the staircase.

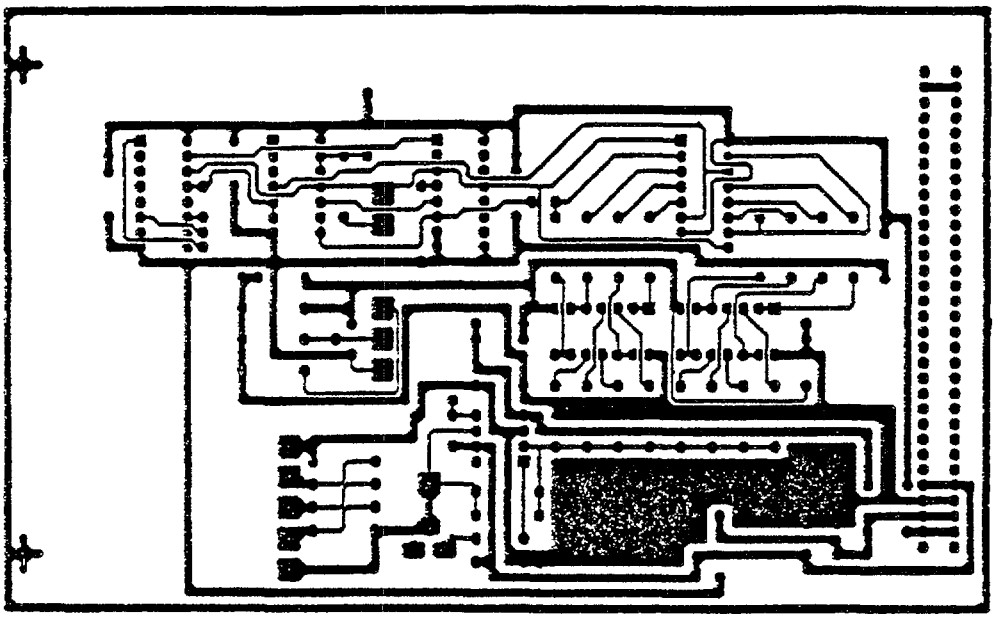
The current switches are just the NAND gates referred above. They are controlled by an 8-bit shift register made with the dual 4-bit registers of the CD4015 package. The shift register input stage is connected to logical state 1, and its clock input is driven by the system clock. The output step time width is, therefore, equal to one clock period. This period can be adjusted between about 2.5 and 50 μs. When the last flip-flop of the shift register changes to state 1, the JK flip-flop (CD4027) is set and, in consequence, the CD4017 counter is reset. This in turn resets the shift register through U7B. The JK flip flop is then reseted, allowing the CD4017 counter to begin counting. When the preset count value is attained, the RST terminal of the shift register is forced LOW, and a new cycle of step generation is initiated.

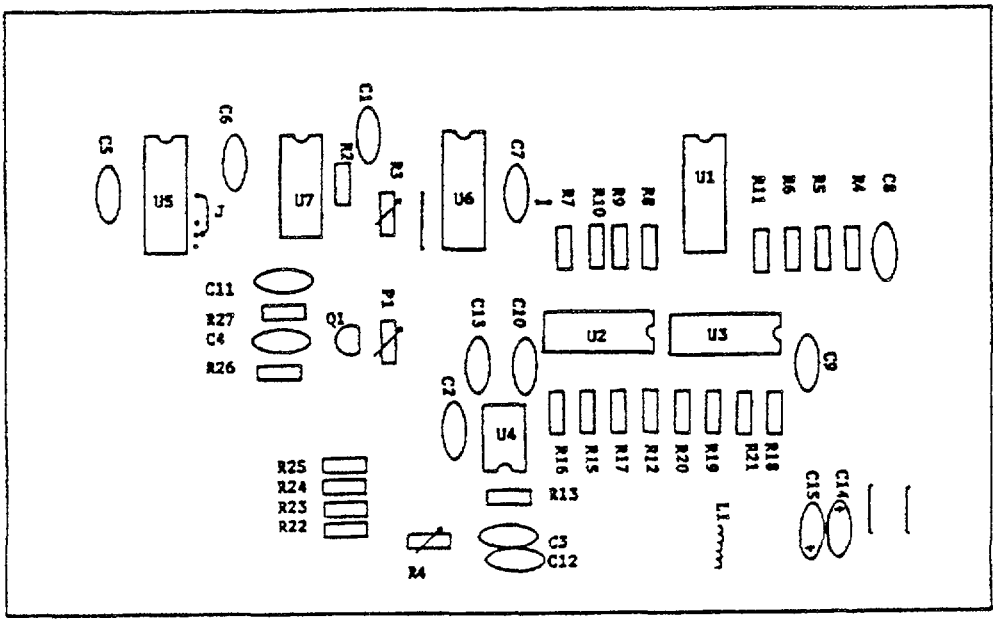
Circuit assembly

The circuit has been assembled in a printed circuit board. The pcb mask and the component lay-out are shown in Fig. 6.7.3.

Fig. 6.7.3

Printer board and compoenents layout for staircase generator.





SPECIAL PROJECT 6.8

SPECTROSCOPY AMPLIFIER

This spectroscopy amplifier is a IAEA modular two width unit. It is constructed on two printed circuit boards; the first with standard EUROCARD format (160 · 100 mm) and the second smaller card (125 ·100 mm), mounted above the first one. The spectroscopy amplifier is powered through the standard 64 pin connector DIN 41612C. It can accept positive input pulses, either in the form of the exponential function with the time constant greater than 25 μs or in the form of step functions superimposed on a ramp voltage (the standard form from an optically coupled, charge sensitive preamplifier). The output pulses are unipolar, semi Gaussian shaped pulses. The pulse shaping is achieved through one approximate differentiation followed by a fourth order complex pole filter, providing highly symmetrical output pulses. Five different time constants are available: 1, 2, 4, 8 and 12 μs. The full width at half maximum is 2.2 ·(the selected time constant). The unipolar output is achieved by using pole/zero cancellation when exponential pulses are applied to the input.

The amplifier has a maximum gain of 2000 with course gains steps of 2000, 1000, 500, 200, 100, 50, 20, and 10. Any gain in between can be selected by a continuous fine gain control in the range from 3 to 1.

In order to maintain the output DC level as close to zero as possible, two DC stabilization feedback loops are introduced. These control loops use the gated integrator circuits.

Block diagram.

The block structure of the amplifier is given in Fig.6.8.1.

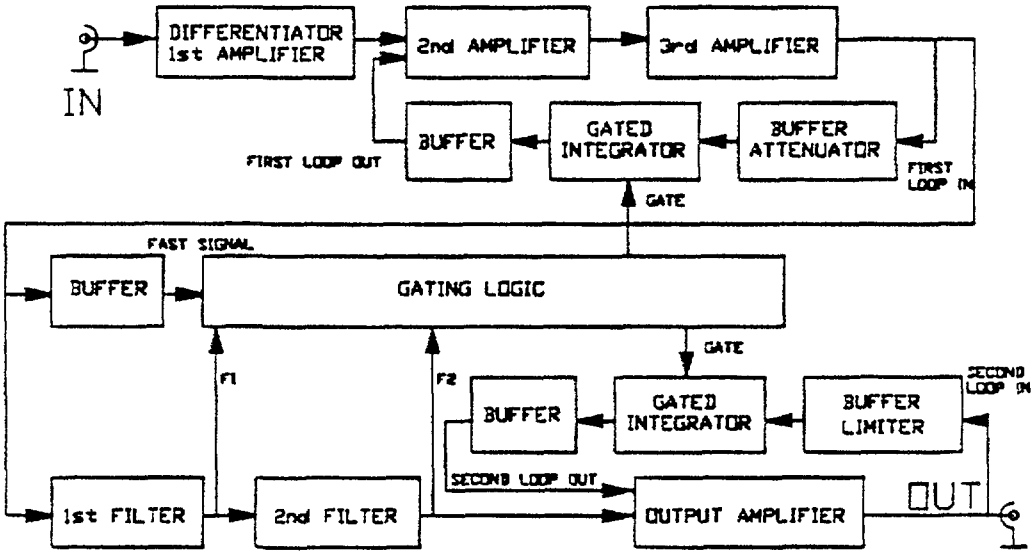
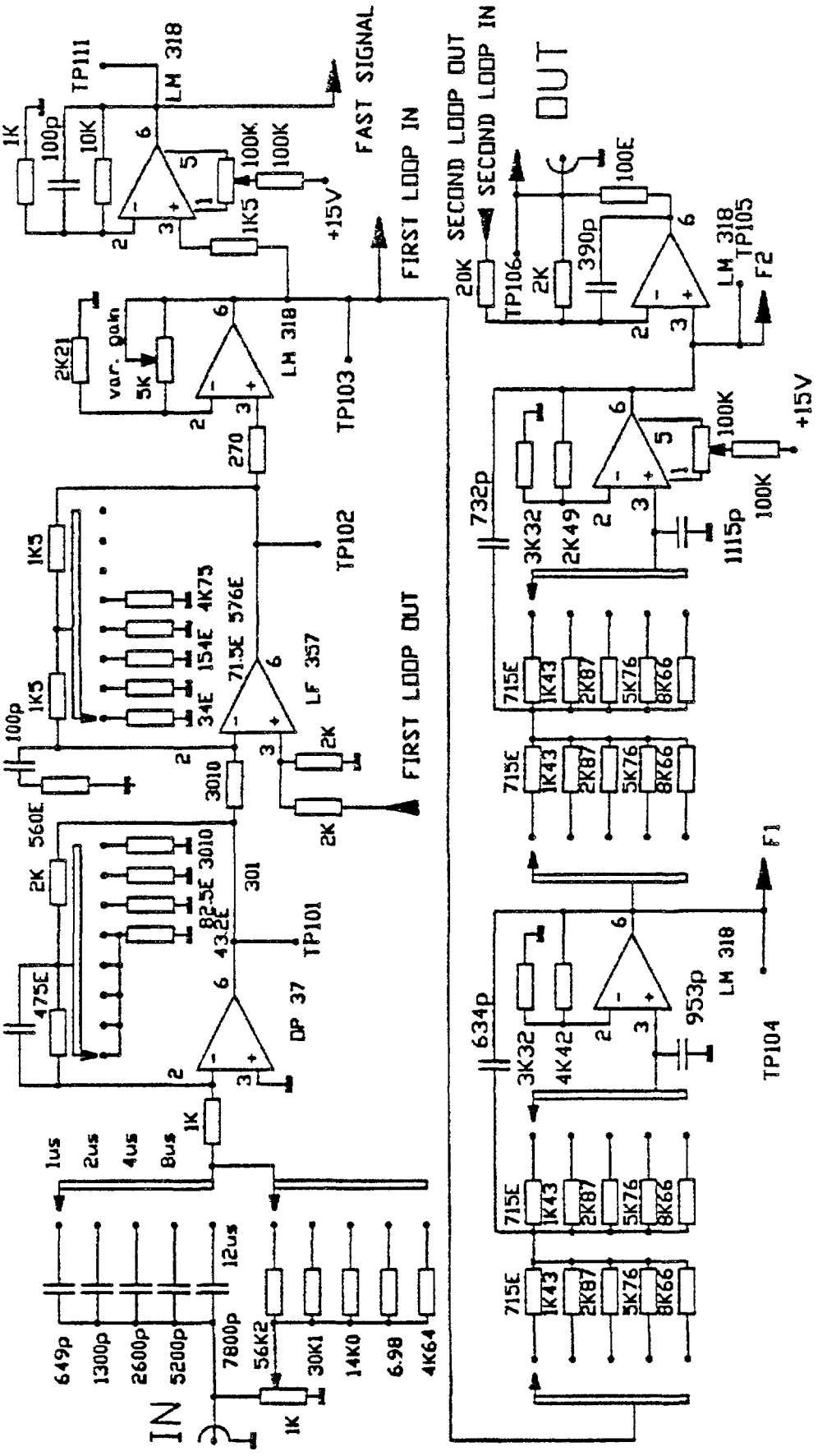


Fig. 6.8.1: Analog processing chain

Fig. 6.8.2:

Analog processing chain: wiring diagram.



The input signal is differentiated, filtered, and amplified in the FIRST AMPLIFIER , working in the inverting configuration. Four coarse gains can be selected. The pole\zero cancellation circuit is also built-in. The SECOND AMPLIFIER, also inverting, has the remaining coarse gain control.

The THIRD AMPLIFIER, in the noninverting configuration includes has the fine gain control using the ten turn front panel potentiometer. Because the DC-coupled chain of three amplifier has an overall gain of more than 1000, the DC shift of the base line could impair normal operation. Therefore, the gated integrator base-line controlling circuit is introduced. To achieve base line restoration, the THIRD AMPLIFIER output signal is applied to the BUFFER ATTENUATOR. The buffered signal is integrated in the GATED INTEGRATOR. Proper gating allows only the base line voltage to be observed. The integration is interrupted in the presence of pulses by the special gating system. As the applied gated integrator has a high output impedance (we use the transconductance operational amplifier with the current output), an additional BUFFER amplifier is used before applying the control voltage to the SECOND AMPLIFIER. The gain of the second and the third AMPLIFIERS is variable; therefore, the properties of the regulation loop i.e. the differentiation constant, would be gain-dependent. To keep the regulation properties at least roughly constant, the BUFFER-ATTENUATOR stage containing the attenuator adequately follows the amplification. The product of the (attenuation) · (amplification) is kept constant. Smaller variations due to the fine gain control do not change the regulation properties appreciably.

The signal from the THIRD AMPLIFIER is applied to a serially connected FIRST and SECOND FILTER and the OUTPUT AMPLIFIER.

The aim of both of the second order complex pole filters is to change the exponentially decaying input pulse curve into a Gaussian shaped pulse.

We are already familiar with many of the basic blocks which are used in the design of this spectroscopy amplifier. Therefore only the new ideas, not discussed before, will be considered in detail.

Main amplifier

The main amplifier is shown in Fig. 6.8.2. The first stage built around an OP37 (ultralow noise operational amplifier) is the approximate differentiator with pole zero cancelation (Experiment 2.6.). Different gains are selected by changing the feedback current. With the unusual layout of three resistors, the stray capacitance problem is solved.

The next stage is a inverting amplifier with an adjustable gain. The same feedback resistor layout used in the preceding stage is used here.

This stage, built around a LM318, is a noninverting amplifier with the fine gain control.

The buffer stage, which provides signals for the control part of the amplifier, is a noninverting amplifier with a gain of 10.

The second order complex pole filtering is achieved in the next two stages (compare Experiment 2.7.).

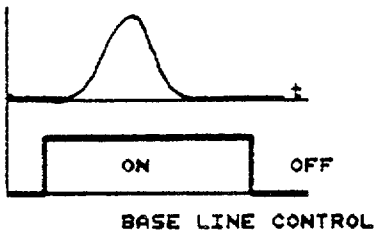
The output stage is a noninverting amplifier with the gain slightly above unity.

Gated integrator base line restorer.

The operation of the gated base line restorer studied in Experiment 2.8 left open the question of how to produce proper gate pulses. The gate pulse must completely cover the full spectroscopy pulse if it is to cut it out and to completely control the base line (Fig. 6.8.3).

Fig. 6.8.3:

Suitable gate pulse.



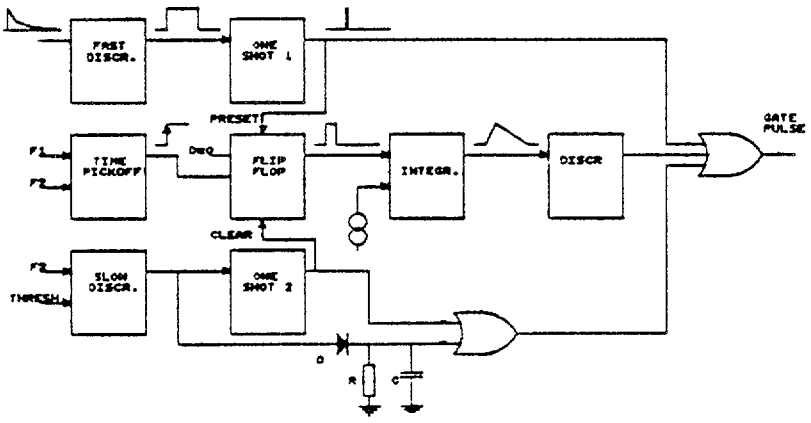
The gate pulse starts when the fast pulse exceeds the fast discriminator threshold voltage. This is early enough to stop the output pulse which delayed at the output because of the filtering. However, the gate pulse should be properly lengthened to eliminate the spectroscopy pulse completely. In principle, the FAST DISCRIMINATOR can trigger a one shot. A one shot provides pulses sufficiently long to eliminate the output pulse. However, the one shot pulse width must be changed simultaneously with the time constant used for the pulse shaping. This is the solution used in all contemporary commercial spectroscopy amplifiers.

In the version described here we use the system that senses the pulse width, and generate a gate pulse matched to the spectroscopy pulses. The idea is explained by using the block diagram (Fig.6.8.4) and the waveforms (Fig.6.8.5). The start of the spectroscopy pulse is sensed by the FAST DISCRIMINATOR triggering the ONE SHOT 1. The FLIPFLOP is then activated, and the logical 1 signal is integrated until the RS flipflop is reset by the TIME PICKOFF. The TIME PICKOFF is a comparator comparing pulses passing the first filter, and the second filter. The time between the FAST DISCRIMINATOR reaction and the moment when both pulses are equal, is proportional to the spectroscopy pulse width. Therefore, the result of the integration is proportional to the spectroscopy pulse width. Now a constant current is connected to the integrator. The integrator output voltage goes down until zero is reached.

The total time while the integrator output voltage was different from zero is proportional to the width of the spectroscopy amplifier output pulse. This time is observed by the zero discriminator which is a part of the gating logic. The discriminator output pulse starts immediately after the time when the FAST DISCRIMINATOR announces the pulse, and stops when pulse is completely over if the discharge current is properly set. However, in practice the response of the DISCRIMINATOR observing the triangular voltage has some delay. For the prompt gate control the ONE SHOT 1 pulse is added to the DISCRIMINATOR pulse using an OR gate.

Fig. 6.8.4:

Generator of gating pulse.



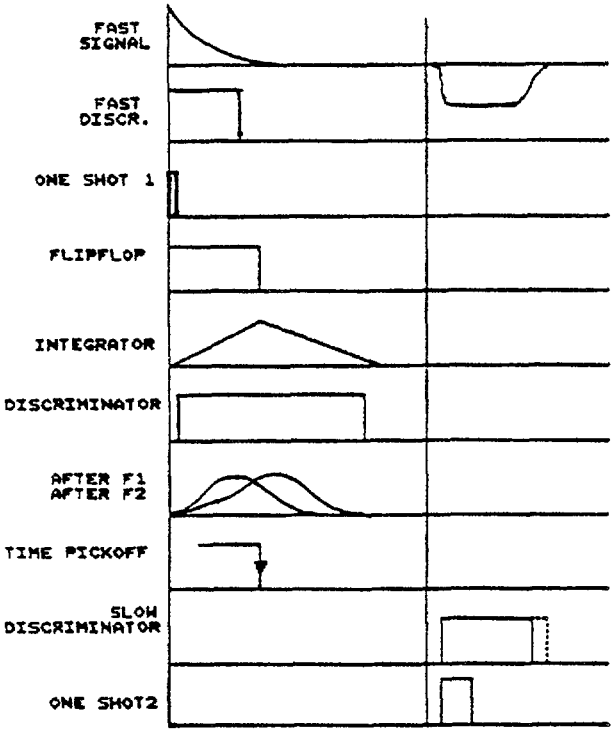


Fig. 6.8.5:

Waveforms in gating pulse generator.

The second type of pulse which should be avoided has a negative polarity. These pulses originate from the optically couples (or any actively coupled) charge sensitive preamplifier, at the time of its discharge. They are much larger than the pulses from the nuclear detector, and badly overload the amplifier. Their arrival is recognized by the SLOW DISCRIMINATOR observing signal after the SECOND FILTER STAGE. In the ONE SHOT 2 and in the NOR GATE, the SLOW COMPARATOR output pulse is prolonged to cover the full duration of the second type of pulses. The wiring diagram of the gate pulse producing circuit is shown in Fig.6.8.6.

Both, the FAST COMPARATOR, and the SLOW COMPARATOR should recognize pulses as quickly as possible. This requires that the discriminator threshold be set slightly above the noise level. The noise level, which depends on the preamplifier selection and the gain used in the spectroscopy amplifier, is sensed automatically through the special built-in unit called the AUTOMATIC THRESHOLD DETECTOR.

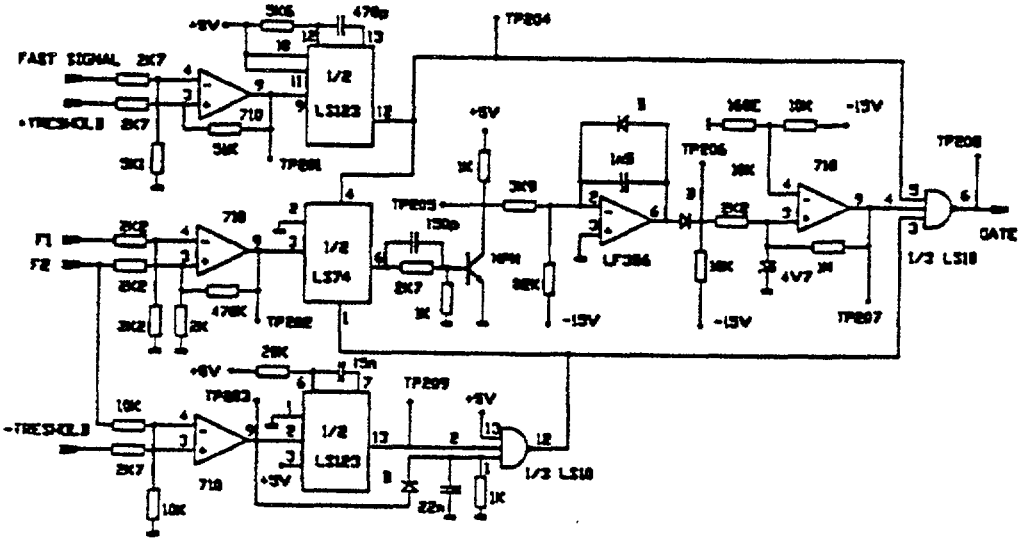


Fig. 6.8.6:

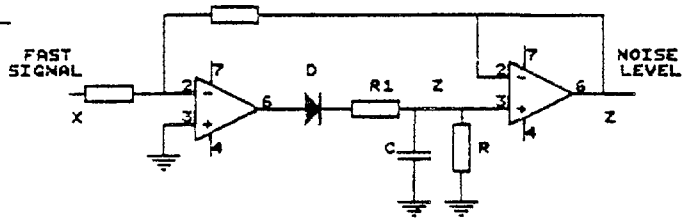
Wiring diagram of gating pulse generator.

Automatic threshold detector

The principles of the automatic threshold detection are explained by using Fig.6.8.7. The fast signal is applied to the input of the comparator. The comparator output charges the capacitor C through the diode D. So far, the circuit is identical with the pulse stretcher described in Experiment 4.1.7. However, in the automatic threshold detector circuit we

Fig. 6.8.7:

Threshold detector.



have added the resistor R in parallel with the capacitor C. The time constant RC is about 0.3 s. The voltage across the capacitor C, z, is repeated at the output of the voltage follower. The output of the voltage follower is compared with the input voltage x. If z is smaller than the input voltage x, then the comparator output voltage will cause the additional charging of the capacitor C. If z is bigger than x, the comparator output voltage will decrease. The diode will be nonconductive but the capacitor will be discharged through the resistor R until both voltages at the comparator input will be the same. Resistor R1 moderates the response of the system to spikes. Voltage across the capacitor follows the noise level of the applied signal. The voltage delivered at the output of the voltage follower is proportional to the noise. It can be used as the threshold voltage of both the FAST and SLOW discriminators. Se Fig.6.8.8 for the detailed wiring diagram.

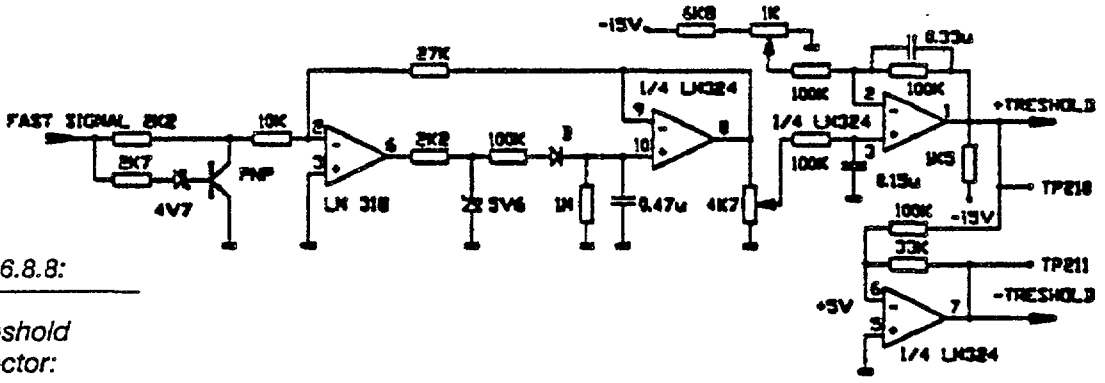


Fig. 6.8.8:

Threshold detector: wiring diagram.

Pileup rejection system.

The pulse pileup effects (Fig.6.8.9) are reduced by the pileup rejection system (PUR). The idea is to interrupt analysis if spectroscopy pulses appears in pairs, too close to each other. Pulses are superimposed, and the observed amplitudes do not correspond to energies of the registered radiation. A simple way to reduce the pileup effect is to stop analysis after each pulse for the time sufficient that the signal amplitude, will reach zero.

Fig. 6.8.9:

Pileup effect.

The pileup rejection used in the present amplifier is shown in Fig 6.8.10. The arrival of each pulse is sensed by the TIME PICKOFF. The arrival time is reported when signal F2 (spectroscopy pulse) pulse drops to 90% if its amplitude. To get this time, we compare F1 and F2 signals. By the comparator transition the RS flipflop is set. It is reset by the end of the gate pulse, from the BLR gating logic unit. The RS flipflop output provides the pile up rejection signal. This signal, applied to the MCA gate input, reject the second pulse when it follows the first pulse too close.

The pileup rejection system has the possibility to combine the generated pileup signal with the inhibit pulse from the charge sensitive preamplifier which is in the normal operating condition applied directly to the gate input of the multichannel analyser.

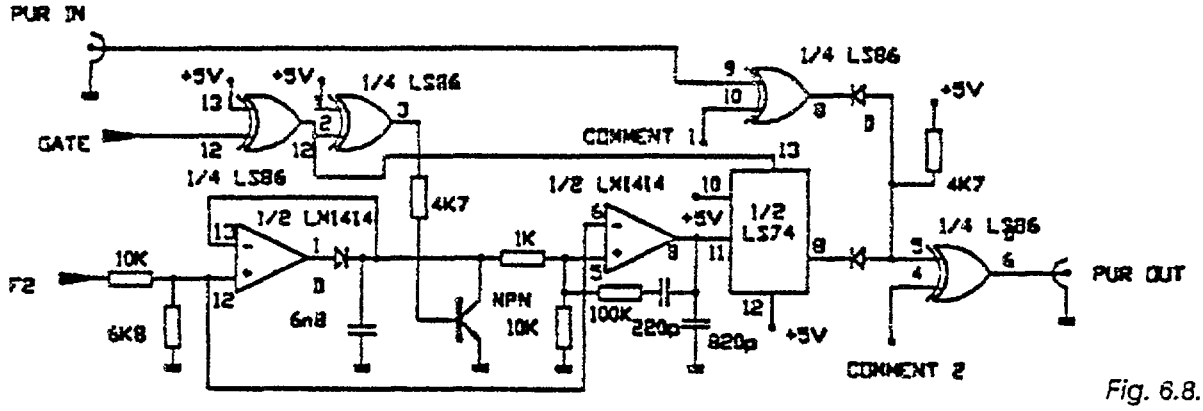


Fig. 6.8.10: Pileup rejector: wiring diagram.

The option is given to select polarity of the input and output pulse. Points marked with COMMENT1 and COMMENT2 should be connected either to ground or to Vcc.

Feedback loops

Both base line controlling feedback loops follow principles presented in Experiment 2.8, but the realization is different (Fig.6.8.11). The integrator using operational amplifier with the FET as the switch is replaced with transconductance amplifier which has the current output (CA3080).

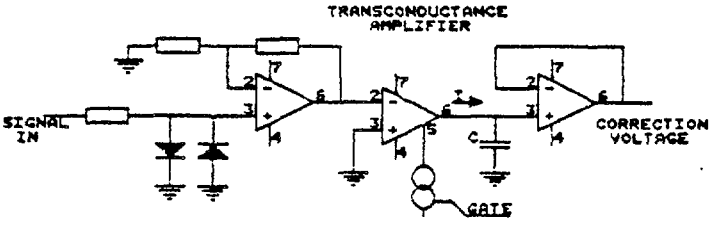


Fig. 6.8.11: Gated integrator.

The gain of the amplifier is determined by current into the control input. If we apply the gated current source, gains 0 or G are achieved when current source is switched on or off. The transconductance amplifier output current is proportional to the input voltage and the control current supplied by the constant current source. This current is integrated in the capacitor C. The resulting voltage is tracked by voltage follower, and used as the offset voltage of the amplifier within the loop.

The wiring diagram of both loops is shown in Fig.6.11.12 and Fig.6.11.13. They are almost identical; the only difference is the voltage attenuator added in the first loop.

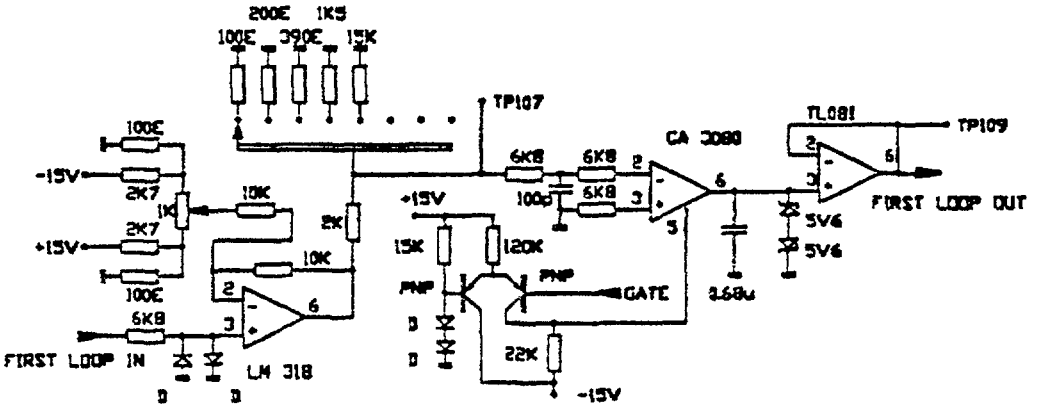
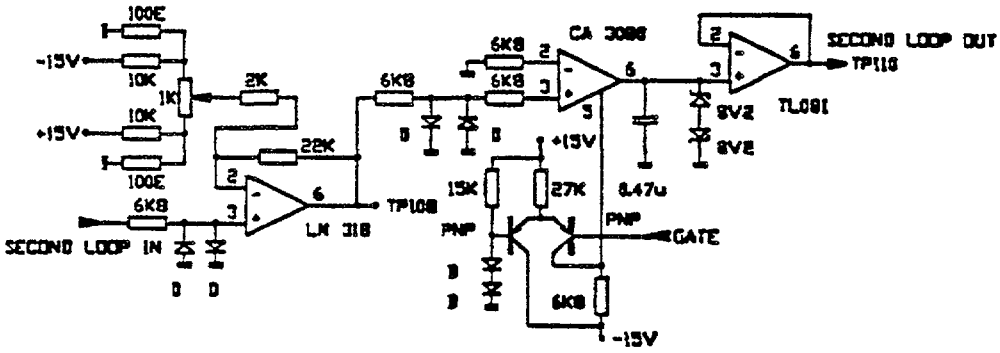


Fig. 6.8.12: First loop.

Fig. 3.8.13:

Second loop.



SPECIAL PROJECT 6.9

SPICE: A SIMULATION PROGRAM FOR ANALOG CIRCUITS

OBJECTIVES

The objective of the present text is to present a computer simulation program for analog circuits. In the design of analog nuclear electronics modules, this programme can be of considerable assistance to the designer. It is advisable to get familiar with such a programme. SPICE is a powerful programme used frequently by professional designers.

REVIEW

Spice is a computer program for circuit analysis and simulation. It will never judge if your circuit is good or bad; it just shows how a particular circuit responds to a defined stimulus. This is exactly what happens with other electronic tools. You may infer from an oscilloscope picture that your circuit is not behaving according to your design goals. That is your conclusion, not the scope's. You must know your trade to take benefit of an hardware tool, such as a scope; and the same applies to software tools, such as Spice.

You may design an analog circuit and check it with Spice before you build a prototype. You may calculate a waveform somewhere in a circuit, and compare that waveform to what you actually observe with a scope in the real circuit. Spice has a companion post-processor program that graphically displays, like a scope does, the waveforms; it even allows you to change, within reasonable limits, the amplitude and time scales of the display without the need to recalculate. We may say that Spice is useful not only for design but also for troubleshooting.

In computer aided design we may indulge in luxuries that would be unreasonable to consider in an hand calculation. To simulate a transistor circuit, for example, Spice does not use the h-parameters or other similar approximations. It uses more complex, more realistic equations. This, of course improves the agreement between the calculated and the observed results.

Spice statements

Spice statements instruct the program to perform various types of analysis. These relate to DC behavior, frequency response and transient response. Noise calculations and Fourier analysis are also included in the program's capabilities. Below is a brief summary of what is done in the various analysis.

In DC analysis, Spice essentially calculates the operating point of the circuit for specified values of the circuit DC sources. All AC sources are nulled. Consider the circuit of Fig.6.9.1.

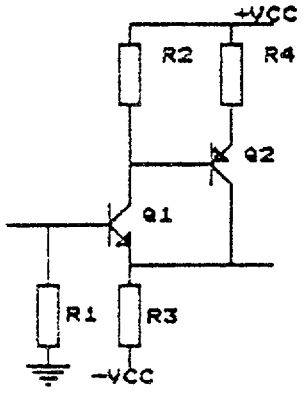


Fig. 5.9.1:

Circuit example.

You may be interested in knowing the current that flows in Q1 and Q2, and the voltage at the emitter of Q1 when the DC voltage at the base of Q1 is swept from -5V to +5V. This is the kind of thing Spice performs if DC analysis is specified; you indicate the source, the limits of the sweep, and the step increase in the voltage from one limit to the other.

Sensitivity analysis is related to DC analysis. Here you instruct Spice to calculate the value of a voltage or current as a function of the value of some component. For example, you may be interested in knowing how the base-emitter voltage of Q1 changes as a function of R2. This allows you to test the effects of a parameter change in circuit performance.

Transfer function analysis is a small signal analysis also related to DC analysis. In transfer analysis you may calculate small signal gain and input or output impedances. Of course, you must tell Spice what you consider to be the input and the output ports; the program has no way to know how the simulated circuit is to be used. The simulation is done essentially by calculating the appropriate derivatives around the operating point.

Frequency response analysis, usually called AC analysis in simulation programs, measures the gain, in both amplitude and phase, between two specified ports. Spice first calculates the DC operating point of the circuit. The parameters describing the circuit components at that point are kept constant while the response to a sinusoidal source is calculated for a number of frequencies inside a specified range. The calculation can be made with any value for the amplitude of the sinusoidal source; the analysis is of the small signal type because the component parameters are kept constant. We obtain the frequency response values by specifying unit amplitude for the source. Thus Spice can produce Bode plots for amplitude and phase; it also calculates group delay. The post processor of Spice allows us to perform a number of mathematical operations with the calculated results. In this way, input and output impedances may be plotted as a function of frequency.

Transient analysis implies the use of time-varying sources. For transient analysis, voltage and current independent sources of various time dependencies are required. Spice has a number of them. You can, further to damped sinusoidal sources, specify exponential waveforms, pulse type waveforms, piecewise linear waveforms. When specifying timings of these waveforms one must always remember that Spice takes the same time to calculate the values at the next time step, whether the step is one second or one nanosecond. For example, if you intend to see what happens when a step voltage is applied to a 10 ms time constant low-pass filter, do not use a pulse with 0.1 ns rise time. Actually, Spice will try to adjust to a reasonable time step automatically (if you do not instruct it otherwise), but will start with step values related to the input signal timing specifications. Transient analysis is certainly the most often required analysis in nuclear electronics circuits.

Transient analysis requires that initial values be given for energy storing components (if not explicitly given they will be assumed to be 0). Also, in circuits such as oscillators, offering Spice an educated guess on the values some of the capacitors will take may save an appreciable calculation time.

Spice is also able to perform Fourier and noise analysis. Fourier analysis essentially gives information on the spectral components of circuit waveforms. Noise analysis takes into account both resistor thermal noise and the noise generated in active devices.

Spice components

Spice built-in models for the usual "linear" passive components (R, C, L, M) are more detailed than the ones normally used in hand calculations. For example, a capacitor is specified by its value at a defined temperature together with linear and quadratic voltage and temperature coefficients.

There are both independent and dependent voltage and current sources. Spice has the whole lot of these dependent,controlled sources: VCCS (voltage controlled current source), VCVS, etc. The value of the source depends polynomially on the value of the controlling variable. Thus one may have either linear or non-linear, polynomial sources. Actually, the polynomial may multidimensional, that is, the source may be controlled by products of circuit current and voltage variables.

Diodes, bipolar and field effect transistors are all defined by a large number of parameter. Device parameters may be kept in a library. For example, Spice will use the appropriate parameters if you specify a transistor as 2N3904 (provided they are in the library). A ancillary program to Spice helps you to define a component from its data sheet specifications.

Spice deals with operational amplifiers and other components, such as transmission lines, as subcircuits. This essentially means that such components are treated as n-terminal devices (for example, 5 terminals for an operational amplifier), the internal circuit of which is defined separately.

Spice circuit description

A circuit is described to Spice by specifying all of its components and the nodes to which they are connected. Like any other computer program, Spice has its own syntax. This, and many other details, we leave for you to read in the program manual. Some of the schematic capture programs, such as Orcad or Schema II, may provide a file that can be used as input for Spice.

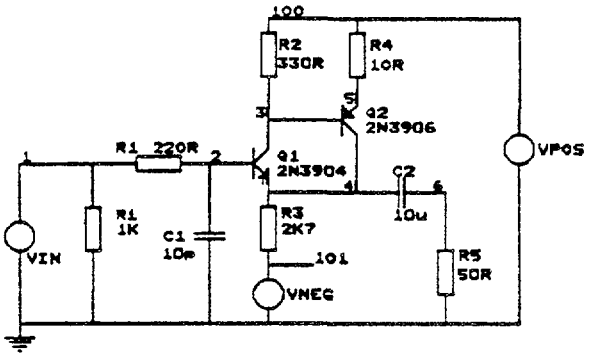
There are in the market other simulation programs different from Spice; a popular example is Microcap. Spice has, however, become a standard. It was developed at the University of California, Berkeley, in the 1970s for mainframe computers. A number of commercial versions are now available for IBM compatible personal computers. The circuit description is similar in all these versions of Spice; they essentially agree with the Berkeley syntax. The example below has been run in PSpice, a program available from MicroSim.

We exemplify a circuit description in Fig.6.9.2. The circuit is similar to the input circuit that is used in some commercially available spectroscopy amplifiers.

Fig. 6.9.2:

PSPICE circuit description.

```
*Voltage follower circuit: PSpice description
Vin   1   0     ac   1    pulse ( 0  1  10n  5n  5n  1u  10u)
Ri    1   0     1k
R1    1   2     220
R2    100  3    330
R3    4    101  2.7k
R4    100  5    10
R5    6    0    50
C1    2    0    10p
C2    4    6    10u
Q1    3    2    4Q2N3904
Q2    4    3    5Q2N3906
Vpos  100  0    12
Vneg  101  0 -12
.DC   Vin  - 1  1    0.1
.AC   dec  10   1k   100meg
.TRAN 1n . 2u
.LIB
.PROBE
.end
```



Special project 6.10

TRANSFER OF SPECTRA DATA

OBJECTIVE

A spectrum will be transfered from a multichannel analyzer to a computer. The technique for moving spectra between two computers with different operating systems will be introduced. A simple programme will be developed in BASIC for reading a spectrum from a MCA and writting it to the hard disk of a PC computer.

REVIEW

In nuclear laboratory, the problem of spectral data transfer in encountered frequently. Such data have to be moved from the MCA to the computer. or from one computer to the other. Some data analysis software have also the programmes for transfer of data. An example is the QXAS (quantitative x-ray analysis) software for DEC Professional computer.

The transfer of files between computers can be implemented in different ways. In case of computers with different operating systems, the KERMIT software offers a easy solution.

To transfer a file from another computer to your MS-DOS driven computer, two versions of KERMIT will be required. In PC-compatible computer, the MS-DOS version has to be installed. For another computer, the user will have to find and install the appropriate version of KERMIT.

The MSKERMIT enables also the file transfer between two MS-DOS operated computers, using a RS232 interface, and a simple cable with four wires connected. This is an inexpensive substitute for users who do not have a local area network available.

The problem in transfer of spectral data from a MCA to a computer is that every manufacturer of stand alone computers uses a different format for storage of spectra. Furthermore, every manufacturer send the data from the MCA to another storage device in a different manner. A programme for data transfer can be designed in such a way that it stores data on the hard disk in the same format as they are coming from the MCA. On the other hand, it might be useful to write the spectrum on the hard disk in such a format that it will be directly readable by the data analysis programme. In such a case, the problem is again the same: every software for data analysis uses a different input format for the spectrum. The issue is further complicated by the fact that the speCtrum is usually equipped with a header that contains information of the real and live time, spectrum name, and much more. The reformatting of such a "header" is as a rule rather complex, as the data in the multichannel manual seldom include information of the contents and format of the header. A partial solution to these problems is the software SPEDAC, developed by the IAEA, that permits the reformatting of spectra from different MCAs to be used with different data analysis programmes.

Experiment 1: Data transfer from MCA to computer

EXPERIMENT

The Canberra 35 PLUS MCA will be used to collect a spectrum in 4096 channels. The spectrum will be transfered to the DEC computer, and stored in a file.

Start by connecting the DEC computer with the MCA. The cable should have four wires, with a female 25 pin connector on both sides. The pins to be used are1,2, 3 and 7, each connected to the corresponding pin on the connector on the other side of the cable.

Next, in DEC activate computer the QXAS software by selecting from the Main Menu the ADDITIONAL APPLICATIONS, and from the second menu the QXAS.

From the QXAS menu select the option "X-ray S35/40 mca data transfer".

The following prompts will have to be answered, as indicated

```
AXIL-EIA

Transfer or retrieve data (T/R) T      (Observe: capital T required.)
Enter spectrum-filename: 002244        (Any number up to 6 digits.)

Now READING spectrum ... please stand by.
```

In case that you made an error, like forgot to, push the buttons READOUT and YES on the MCA, the unpleasant message will appear

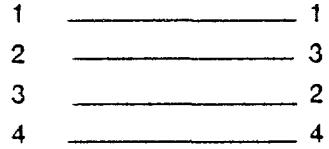
```
FATAL I/O ERROR .... press RESUME to continue
```

If the transfer was successful, the appropriate message will make you happy. Now, you have in the current directory of DEC the spectrum marked with the selected filename. It can be used in the analysis programme of QXAS.

Experiment 2: Use of KERMIT

The spectrum transferred from the MCA will now be send to a PC computer.

Hardware installation. The computers to be used in this experiment are a DEC Professional 350 and an PC-compatible. The DEC uses the P/OS operating system (a child of the operating systems used with PDP series fop computers). The PC uses DOS.



These computers will be connected via the RS232 serial interface. A cable should be made, having a female 25-pin D25 connector on one side, and a 9-pin female connector on the other. Four wires will be connected as indicated below.

Software installation. The KERMIT programmes have to be installed in both computers. Make directories with suitable names, and copy the necessary files from the floppy disks. In the DEC computer, this is done by using the DISK services, and selecting the INSTALL APPLICATION OPTION. IN THE dos computer, the file MSKERMIT should be copied to the hard disk.

Operation. KERMIT should be started on both computer by appropriate command. In DEC, the ADDITIONAL APPLICATION should be selected from the main menu, and the KERMIT from the second menu. The prompt of KERMIT will appear

```
$KERMIT-11
```

We can decide that the DEC computer will be the pasive one. i.e. all the command for data transfer we will issue from the PC. We will have to tell the DEC computer this, and also have to specify the rate of transfer, The following three commands will do the job

```
$KERMIT-11setspeed9600
$KERMIT-11 set duplex half
$KERMIT-11 server
```

Next, we have to prepare the PC for KERMIT operations. The following command will have to be issued (note the prompts for KERMIT on PC computer!) to prepare the computer for operation at the correctly transfer rate m i.e. 9600 bauds:

```
Kermit-MSsetspeed9600
```

Note: if you type "?" at the kermit prompt you will get on the screen the list of all the possible commands (see Appendix I to this experiment).

Both machines can act as server or controller, for this example we assume that the DEC PRO will be the server.

The student may try at different speeds to get the most efficient transmission speed. Hint: Try also 19200 bauds and 38200 bauds.

Experiment 3: Spectrum reformatting

The spectrum transferred from the DEC top the PC should be reformatted , so that it can be used in the SPAN (a programme for neutron activation analysis) programme, installed in the PC. The software package SPEDAC will be used.

Start the programme by typing:

```
C: SPEDAC
```

The menu will permit you to select the present format of the spectrum, and the new format. In a number of intereactive frames, you can define the correct procedure (see the SPEDAC Manual).

The reformatted spectrum can be displayed with the graphics faciltities of the SPAN software.

Experiment 4: Software for spectrum transfer from a MCA

For the example of a spectrum transfer programme, we will select the same spectrum on the Canberra 35 PLUS MCA as in the first experiment. However, now we will develop a computer programme that will do the transfer directly. The tranfer programme will be written in QUICK BASIC. A stepwise instruction for development of the programme is given below, for a programme that permits the transfer of 1024 channels, and stores the spectrum file on a harddisk of floppy disk, in ASCII format suitable as direct input to the QXAS programme for x-ray analysis.

The programme is build up gradually, each step is extensively commented.

```
'Programme for transfer of spectral data from a MCA of the type
'Canberra series 35, 35PLUS or 40

DIM spec(4100)                    A suitable table dimensioning of the expected data
                                  is made by this line

CLS                               The screen is cleared
LOCATE 10, 5                      Position on the screen is defined

PRINT "Transfer MCA to computer"
            This text will appear on the screen in specified position


LOCATE 11,5
PRINT "-------------------------"
LOCATE 13, 5
PRINT "Press READOUT and YES on MCA"     These are instructions for
                                         operator, what to do at the MCA side

LOCATE 14, 5
PRINT "Mode ASCII, full MEMORY"

                                  Next we will intialize the start of the transfer.
                                  permitting maximum of 10 seconds for
                                  operator to start the MCA

OPEN "COM2: 4800 ,N ,8 ,1 ,ASC, cd10000" FOR INPUT AS 3 LEN = 1024

                                  The input conditions are specified:
                                  -COM2 defines the communication serial port number 2
                                  - 4800 baud rate
                                  - N no parity option is selected
                                  - 8 each word is 8 bits
                                  - 1 number of stop bits
```

```
                                    - ASC    ASCII mode
                                    - cd10000  wait for up to 10 seconds
                                    - LEN = 1024 defines the maximum length of the
                                      communications buffer

sp% = 1                             Initilizes counter to get the number of channels
                                                and store data in the spectrum vector
CLS Clears the screen

LOCATE 16, 5                                    Tell the user that data is coming in
PRINT "Receiving data ...."

receive:                        Label that begins loop for receiving channl one by one
a$ = INPUT$(1, 3)                    Get a character from the communications buffer
```

On Canberra MCS the format of spectra data is as follows:

CHR$(15)nnnnnnnn

where n represents and ASCII digit and the 8 n's are the contents of a channel with leading spaces.

The next part of the programme looks for the tags in the incoming data and selects spectral data from the information arriving from the MCA.

```
WHILE (ASC(a$) 15)                                  Find the start of one channel
 IF (ASC(a$) = 4) THEN GOTO spend                   Test the end of spectrum
   CHR$(4)=End of Transmission                                          (EOT)

repeat:                                          Label for loop to wait for one character.

IF (LOC(3) 0) THEN                          Test if there are characters in the buffer
  a$ = INPUT$(1, #3)                                              If so, get one
ELSE
GOTO repeat                                                       If not , wait
END IF
WEND                                          Loop until a start of channel data arrives

WHILE (LOC(3) 8)                    This loop waits until all the data for one channel
WEND                                                          has been received


b$ = INPUT$(8, #3)                          Transfers the data to an string variable
spec(sp%) = VAL(b$)                  Gets the value from the string variable and
                                                  stores it in the spectrum vector.
```

```
sp% = sp% + 1                                    Increments counter by 1
GOTO receive                                     Go to receive next channel
spent #3
CLOSE #3                                  Close comunnication channel and release buffers
CLS                                     Tell the user that all the data have been transferred

LOCATE 16,5
PRINT "Transfer complete"
LOCATE 18,5
INPUT "Enter file name to store spectrum "; file$
OPEN file$ FOR OUTPUT AS #2                      Open a disk file for writing data

PRINT #2, "$SPEC_ID:"                            Write a spectrum file header
PRINT #2, file$
day$ =DATE$                                  You should take care to write the labels
hour$ = TIME$ like $SPEC_ID                                precisely as they are.
PRINT #2, "$DATE_MEA:"                          If you don't programmes for data
                                      processing or reformating will not be able to use it.
PRINT #2, day$; " "; hour$
timtot = spec(2)                    Separate total and live time in spectra data, and
timliv = spec(1)                                                        write them
spec(1) = 0
spec(2) = 0
PRINT #2, "MEAS_TIM:"
PRINT #2, USING "###### ######"; timliv, timtot

PRINT #2, "$DATA:"                               Finally, write spectral data
PRINT #2, USING "######### #########"; 0, sp% - 2      Write first and last
                                                                  channel number
FOR i% = 1 TO sp% - 1                            Write the contents of all the
                                          channels in lines with 10 channels each
PRINT #2, USING "########"; spec(i%);
IF (INT(i% / 10) * 10 = i%) THEN
  PRINT #2,                                  Begin a new line every 10 channels
END IF
NEXT i%
CLOSE #2                                                 Close the spectrum file
END
```

After succesfully running this programme and checking the results by plotting the spectrum on the screen using either QXAS or SPEDAC software packages the student should be able to write a programme that takes an spectrum from disk and sends it back to the MCA.

On the MCA side you should press READ IN, select EIA and press YES in order to set it to receive data

Hints for sending data to an MCA.

First read the spectrum from disk to a properly dimensioned internal BASIC vector.

```
OPEN file$ FOR INPUT AS #2
DO
LINE INPUT #2, line$
LOOP UNTIL (line$ = "$DATA:")
INPUT #2, first%, last%
FOR i% = first% TO last%
INPUT #2, spec(i%)
NEXT
CLOSE #2
```

Then you should open a communications channel to send data

```
OPEN "COM2: 4800,N,8,1,asc" FOR OUTPUT AS #1
```

Then send the address of the first channel to the MCA, preceeded by the apropriate control character and the necessary leading spaces.
The format for an address is the following: CHR$(27)nnnnn

```
num$ = STR$(first%)
l% = LEN(num$)
sp$ = SPACE$(8 - l%)
data$ = CHR$(27) + sp$ + num$
PRINT #1, data$
```

Then send the channels one by one in the already discussed format including the control character.

```
num$ = STR$(spec(i%))
l% = LEN(num$)
sp$ = SPACE$(8 - l%)
datos$ = CHR$(15) + sp$ + num$
PRINT #1, datos$
```

Finaly send an end of transmision (EOT) character so that the MCA exits from the data read-in mode.

```
PRINT #1, CHR$(4)
```

Notes:

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